EUROPEAN EDITION

# EDN®

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS WORLDWIDE

PROCESSOR UPDATES PG 65

22 FEB 1993

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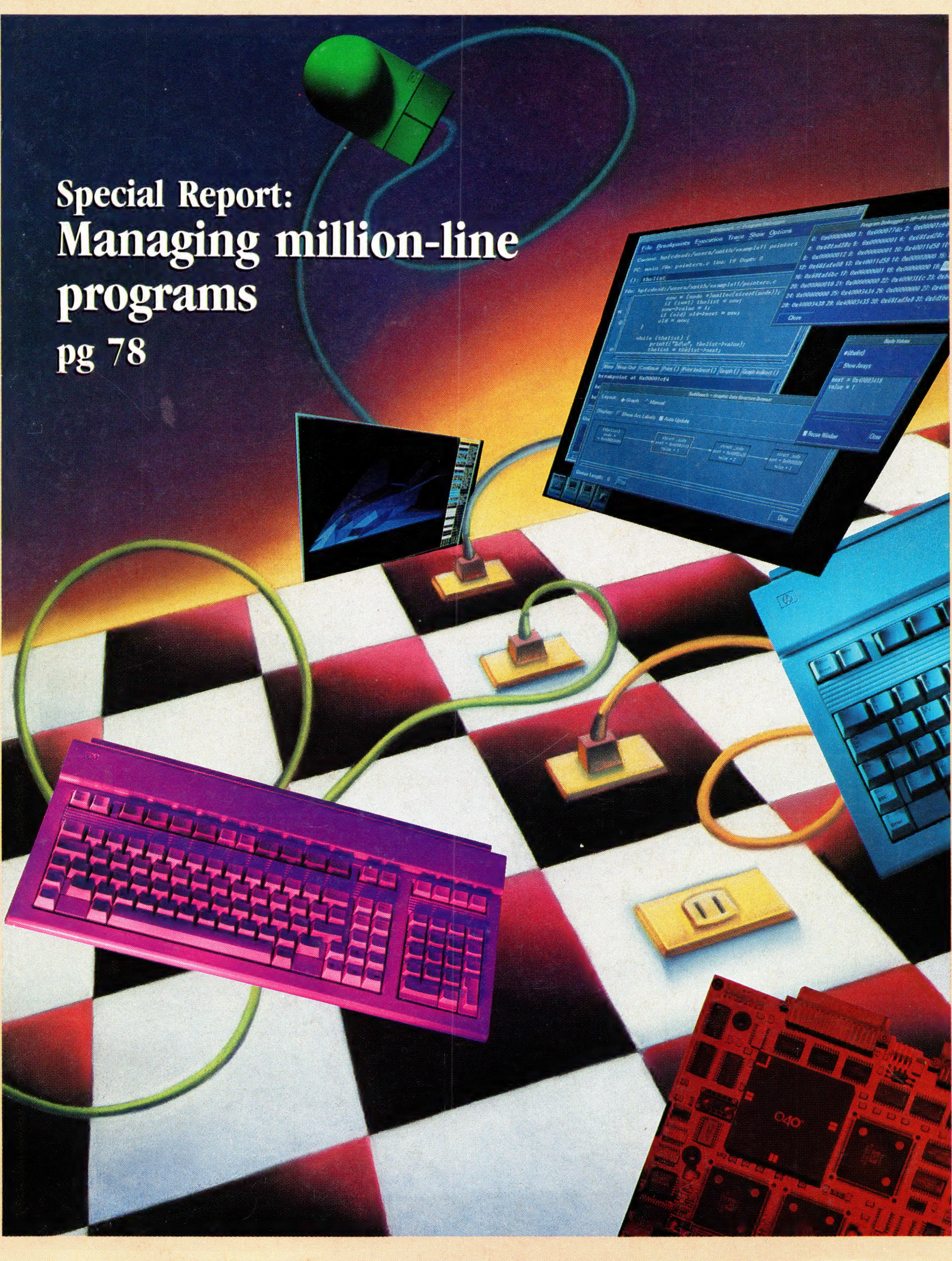
February 4, 1993



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Managing million-line programs
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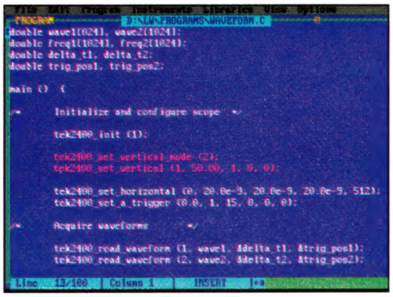
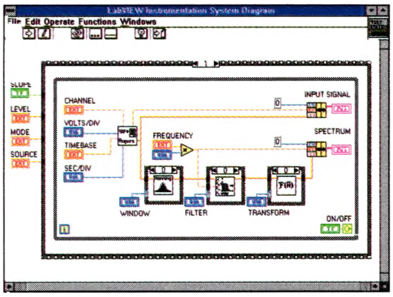

File Edit Program Instruments Libraries View Options
PROGRAM
D:\LW\PROGRAMS\WAVEFORM.C
Line 13/100
Column 1
INSERT

```
double wave1[1024], wave2[1024];
double freq1[1024], freq2[1024];
double delta_t1, delta_t2;
double trig_pos1, trig_pos2;

main ()  {

/*      Initialize and configure scope  */

        tek2400_init (1);

        tek2400_set_vertical_mode (2);
        tek2400_set_vertical (1, 50.00, 1, 0, 0);

        tek2400_set_horizontal (0, 20.0e-9, 20.0e-9, 20.0e-9, 512);
        tek2400_set_a_trigger (0.0, 1, 15, 0, 0, 0);

/*      Acquire waveforms          */

        tek2400_read_waveform (1, wave1, &delta_t1, &trig_pos1);
        tek2400_read_waveform (2, wave2, &delta_t2, &trig_pos2);
```



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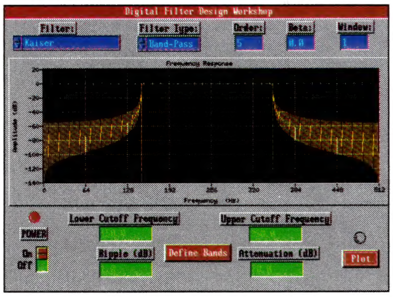

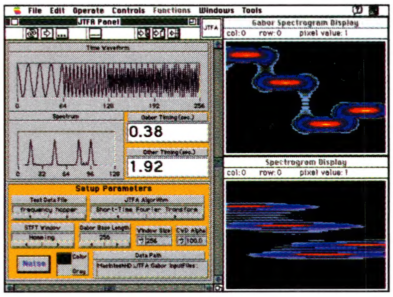

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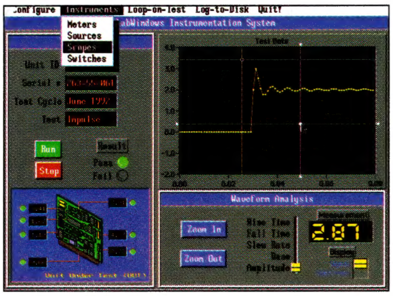

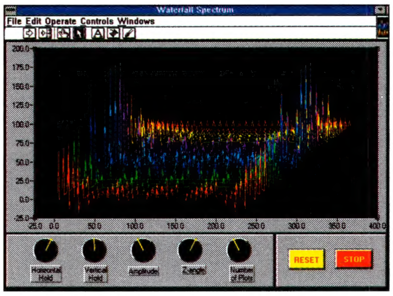

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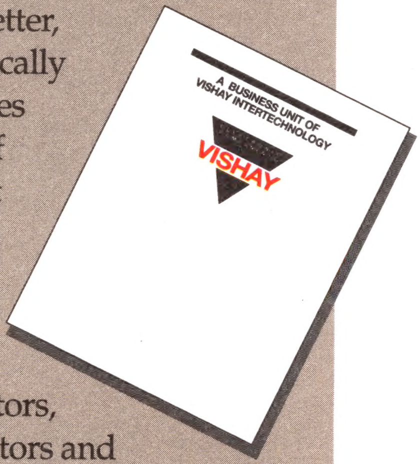

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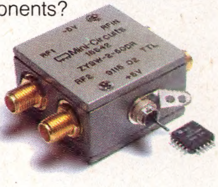

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| RF Input (max dBm) | — | 20 | — | 22 | 22 | 26 |
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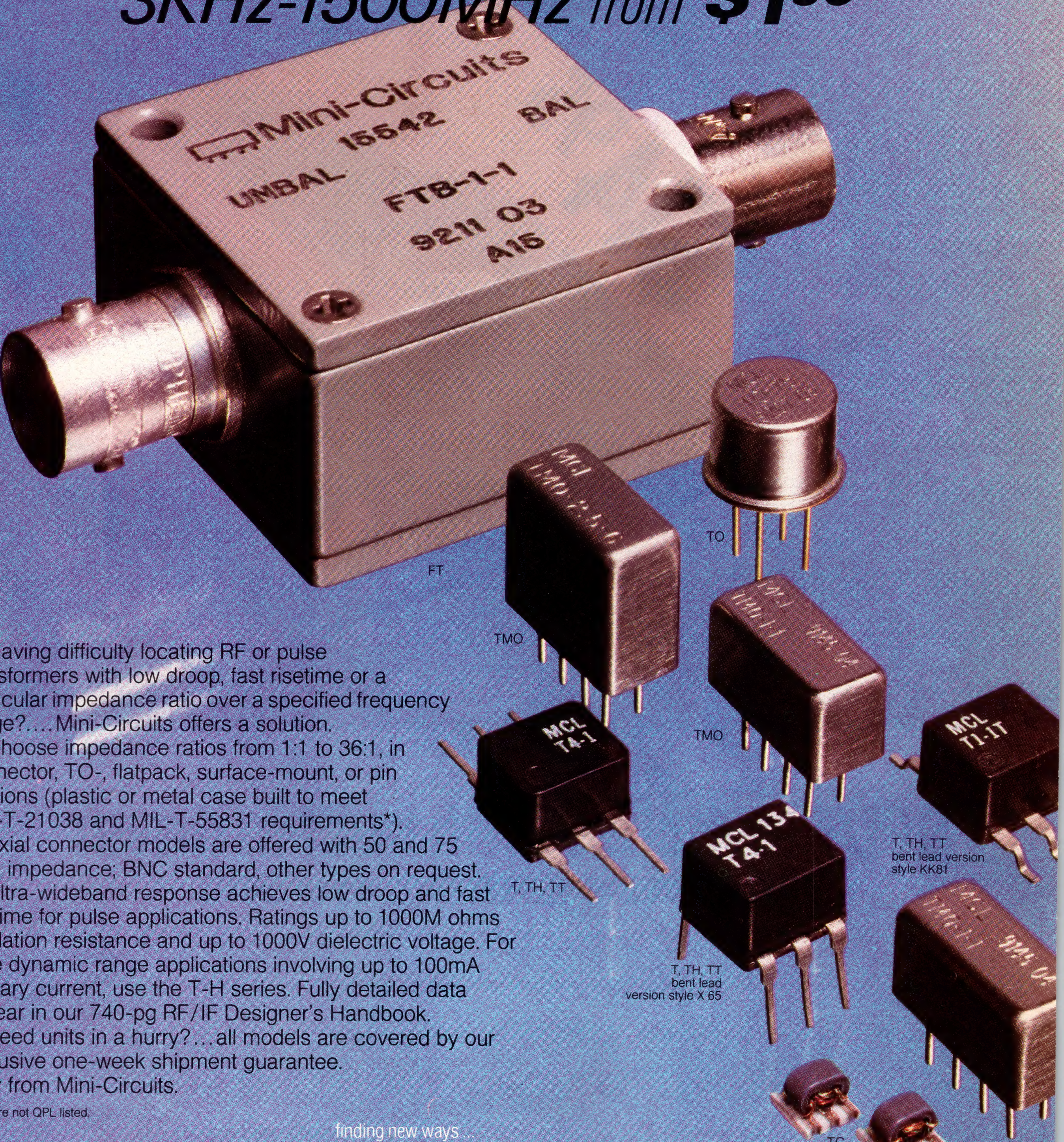

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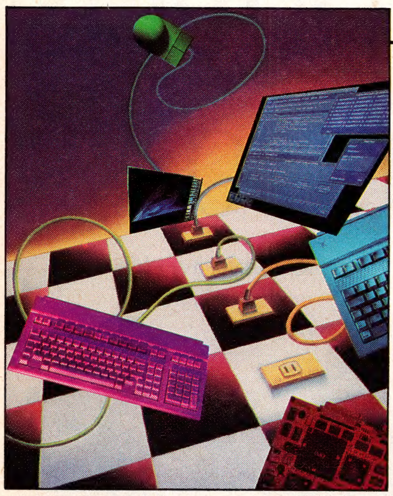

**On the cover:** You can't play games when programming millions of lines of code; big software projects often demand many different tools and lots of personnel. Bringing your project to successful completion requires the right tools, knowledge, and more than a little organization. (Photo courtesy Hewlett-Packard's Software Engineering Systems Div) . . . . . . . . . . . . . **PAGE 78**

SPECIAL REPORT

**Staying afloat in high software seas**

Million-line software projects differ from small ones, and not just in line count for code and head count for the development team. You need additional tools and a new set of rules.—*John C Napier, Technical Editor* **78**

SPECIAL PROJECT

**EDN Hands-On VHDL Design Project**
**Writing the Code**

Having selected the Z80, and with the design center set up, the author begins to write the model.
—*Michael C Markowitz, Editor, EDN Asia* **94**

DESIGN FEATURE

**Getting the most out of redundant arrays of inexpensive disks**

Large databases demand fault tolerance. Redundant arrays of inexpensive disks (RAIDs) can deliver, but first you've got to choose an architecture.
—*John McBride, Hewlett-Packard Co* **109**

TECHNOLOGY UPDATE

**External power supplies enhance system design options**

External power supplies are being accepted as the primary power source for a variety of advanced products.—*Tom Ormond, Senior Technical Editor* **39**

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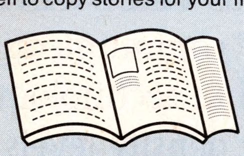
Turn to the last information-retrieval service card in the back of this magazine and you'll find a foldout table of contents. Now, instead of flipping back and forth from this table of contents to the articles you want to read, you can have the convenient foldout open at all times while you're reading EDN. Use the foldout contents to mark off articles you'd like your colleagues to read or to remind yourself to copy stories for your files.



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**February 4, 1993**

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## TECHNOLOGY UPDATE

### Boost programmable logic performance with timing-driven tools

The best way to avoid timing problems at the end of a design is to use tools and methods from the start that help you meet your timing constraints.—*Doug Conner, Technical Editor*

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# INSIDE EDN

## A summary and analysis of articles in this issue

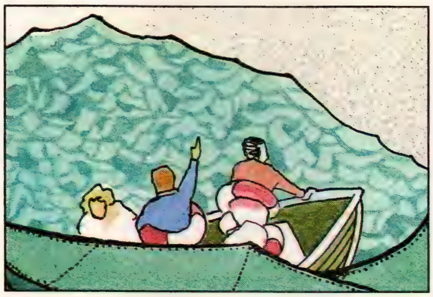
Complexity adds a new dimension to any project—whether you're working on a massive software program, a microprocessor design, or complex-PLD timing problems. For example, **writing a million-line program** isn't like writing a hundred 10,000-line programs, says John Napier in this issue's cover story. If you're part of a team writing a really big program, you'll find yourself using tools to track system requirements, manage documentation, link software modules, and browse and search code modules for a specific type of information, such as classes or function names. You'll also need tools just to communicate effectively with your team members.

To illustrate these points, John describes the efforts behind four really big programs: a PC-based CAE tool, a workstation-based CAE tool, software that runs a warship, and software that pilots a commercial airliner.

Mike Markowitz, in part 3 of his quest to **design the Z80 using VHDL** (VHSIC Hardware Description Language), describes creating, writing, and debugging the model. He had already figured out his modeling strategy, but had difficulty doing what he wanted to do, "How do I say something in VHDL so that the compiler will understand it, and it will match the test pattern? Learning VHDL is like learning to speak a foreign language. I could put together a sentence, but not a paragraph."

During this stage of the game, Mike fell prey to the engineer's tendency to look for elegant solutions instead of simple ones. For example, an instruction group of exchange operations swaps the contents of two registers in one clock cycle. Mike sweated over finding a way for 96 bits to travel over the 8-bit bus in one clock cycle until Steve Leibson pointed out that the data didn't have to move—Mike could rename the registers instead.

Mike—and probably everyone else—would like to get better performance with less effort. Doug Conner says that's what you'll get by using timing tools to design FPGAs and complex PLDs. **Programmable-logic timing tools** can flag timing problems early so you can find and resolve these problems earlier in a design. Even if these tools fail to meet your timing constraints, they'll still flag problems so you'll immediately know where the trouble is. Currently, most programmable-logic design tools are not timing-driven, but Doug expects more to appear this year.



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In another staff-written story, Tom Ormond dispels the notion that **external power supplies** are technically inferior to internal supplies and only good for consumer products. As demand increases for smaller and lighter products, external supplies are turning up in a variety of advanced products. Using external supplies simplifies a design, reduces heat production, and eliminates a source of hazardous voltage and magnetic interference from the enclosure. And don't forget cost. External supplies reduce assembly and product-development costs, and manufacturers can often deliver stand-alone power supplies for less than an OEM would spend to build a supply into its product.

**Julie Anne Schofield**
**Senior Associate Editor**

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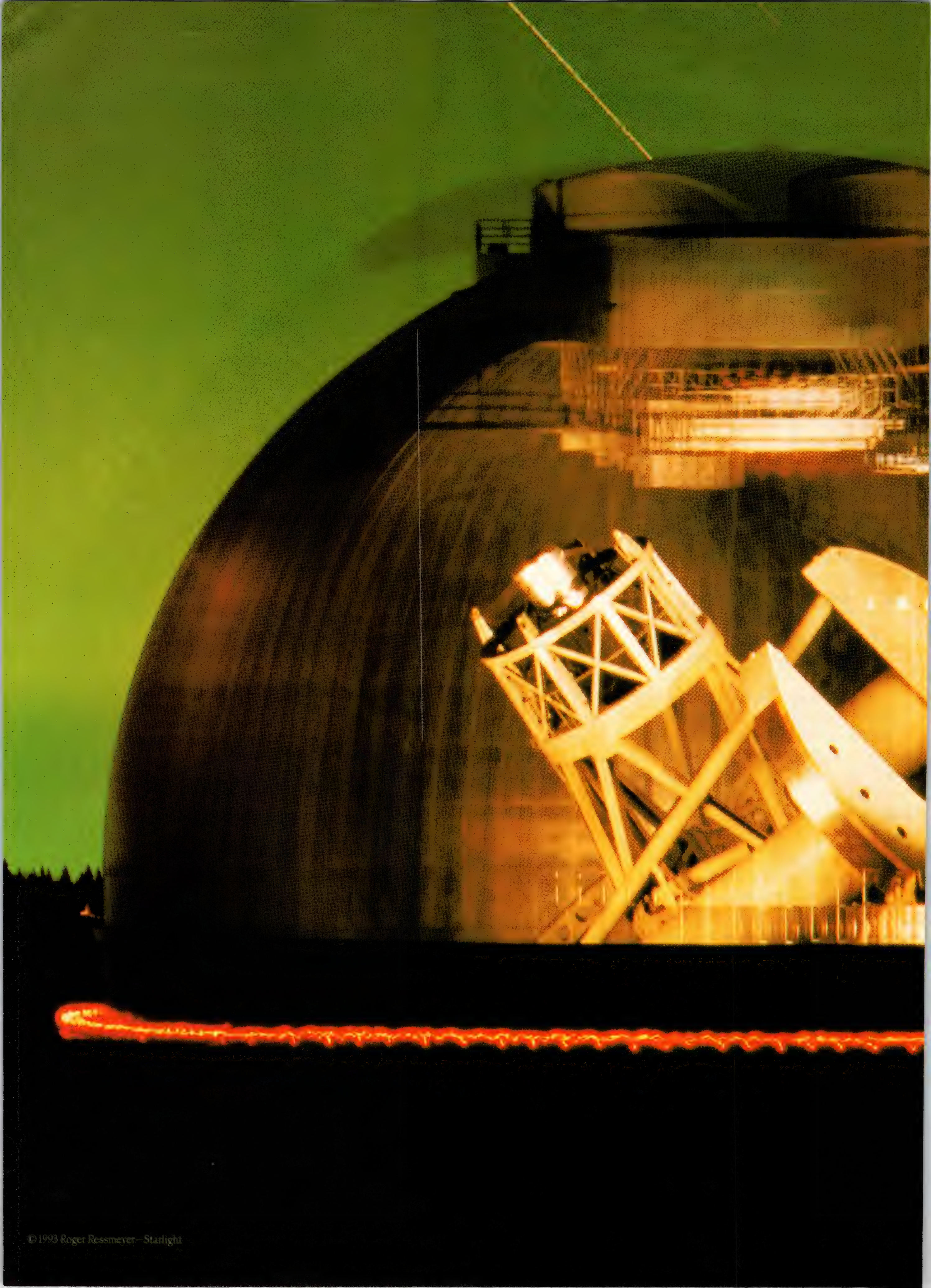

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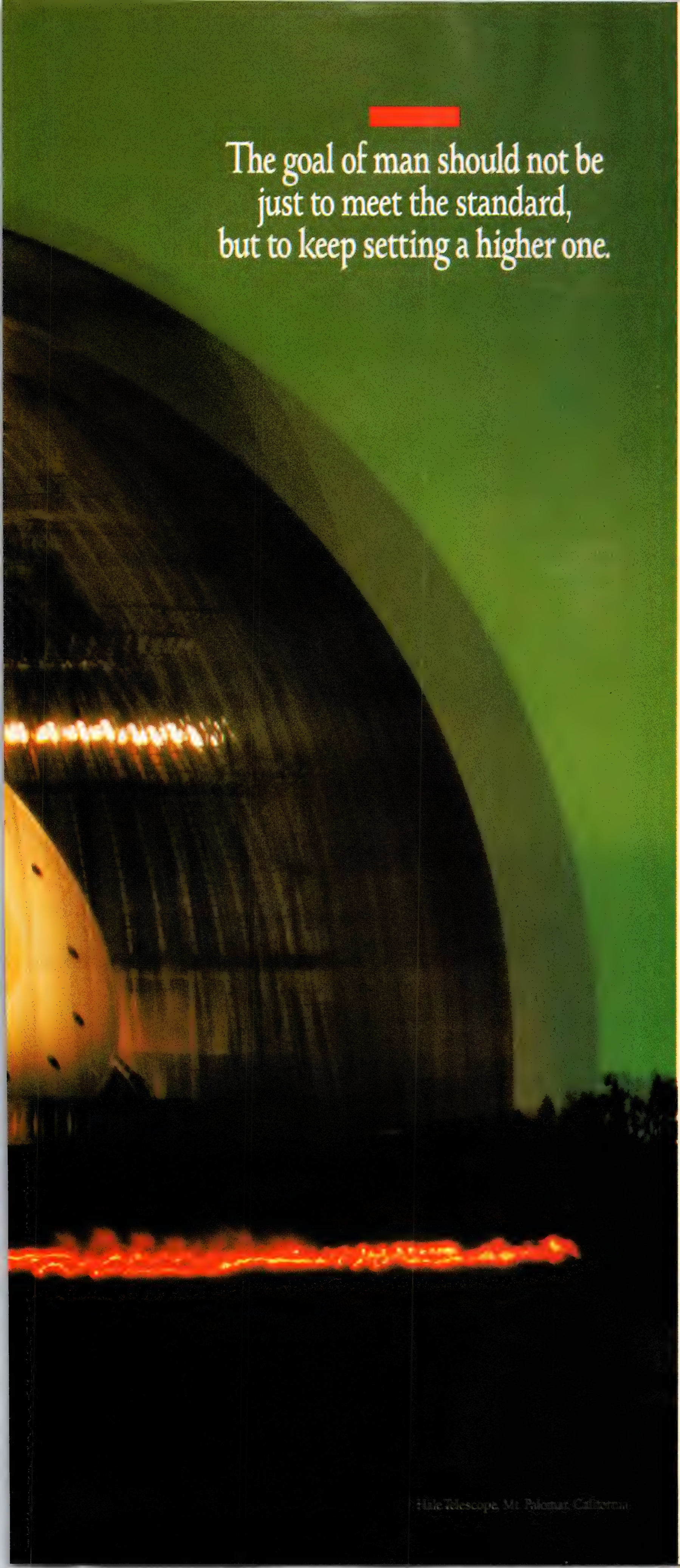
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but to keep setting a higher one.
Hale Telescope, Mt. Palomar, California

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**CIRCLE NO. 16**

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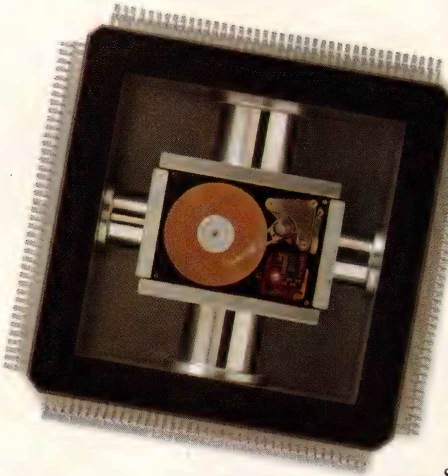

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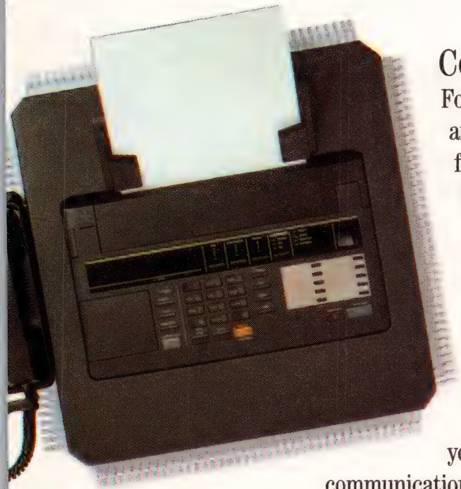

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CIRCLE NO. 18

# Silicon tackles RF wireless communications applications

National Semiconductor is leveraging its LAN communications expertise and an advanced BiCMOS process to enter the wireless communications market. The first product in this line of silicon-based RF (radio frequency) ICs is a family of phase-locked-loop frequency synthesizers that operate as fast as 2.5 GHz. The product family is based on National's ABIC-IV BiCMOS process, which achieves a transistor toggle frequency ($f_t$) of 14 GHz.

The PLL family comprises four members: the LMX-1501A, -1511, -2315, and -2320. Each has a reference oscillator, two programmable counters, a prescaler, a phase comparator, and a charge pump integrated on chip. The charge pump's output can drive a VCO (voltage-controlled oscillator), or you can use the output signals from the comparator to drive an external charge pump. The devices are programmable through a 3-wire serial interface and can operate from 2.7 to 5.5V.

The two programmable counters divide the reference clock and the VCO's output signal before presentation to the phase comparator so that the VCO's frequency becomes a rational multiple of the reference frequency. To provide a range of VCO output frequency settings, a 14-bit counter works on the reference clock, and an 18-bit counter works on the VCO signal. The maximum VCO frequency the devices can accept ranges from 1.1 to 2 GHz.

The LMX1501A, -1511, and -2315 operate at 1.1 GHz; the -2320 operates at 2 GHz. Each consumes 18 mW at 3V. Additionally, the LMX23xx devices offer power-down modes that reduce their standby power to 300 μW. The devices come in a variety of plastic-package types, including small-outline (SO) and thin shrink small-outline-package (TSSOP) styles, and will be in production by March. Prices range from $4.25 (100). National Semiconductor, Santa Clara, CA, (408) 721-5000.

—by Richard A Quinnell

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# Pick up your Innovation nomination packets

Each year, EDN recognizes achievement in the electronics industry by sponsoring the Innovation and Innovator of the Year Awards. It's time again to start thinking about products released between March 31, 1992, and March 31, 1993, as well as the people behind those products, that deserve recognition for this year's award. Innovation awards are presented for nine major product categories—ICs and semiconductors, microprocessors, test and measurement, CAE/CAD, computers and peripherals, components, hardware and interconnect, software, and power sources—and Innovator of the Year.

EDN encourages you to complete a nomination packet and let us know which products—and designers—are outstanding candidates for these awards. Applications are due on or before March 26, 1993. To receive a nomination packet, contact Kathy Calderini, EDN, 275 Washington St, Newton, MA 02158, (617) 558-4526, FAX (617) 558-4470.

—by Susan Rose

# Arbitrary waveform generator offers large memory

The 2414A arbitrary waveform generator from Pragmatic Instruments offers 12-bit resolution and a 160k-word memory with sampling rates from 0.1 Hz to 20 MHz. You can choose from 20 standard waveforms or create your own using a mouse, a PC, or downloading from a digital storage oscilloscope. The instrument costs $2945, including an RS-232C interface and software. Options include an IEEE-488.2 interface ($495) and a waveform sequence generator ($895) that lets you string together as many as 1000 waveforms and repeat them. Pragmatic Instruments Inc, San Diego, CA, (619) 271-6770, FAX (619) 271-9567.

—by Doug Conner

# Dual-disk drive doubles PCMCIA card capacity

Maxtor Corp's disk drive in a PCMCIA (Personal Computer Memory Card International Association) Type III package brings desktop applications to portable computers in a removable module. The MXL-105-III uses two disks (four data surfaces) to create a storage capacity of 105 Mbytes, which is enough to run Windows and a selection of commonly used applications programs. The top capacity for other PCMCIA-compliant drives is 40 to 60 Mbytes. Some higher-capacity drives fit within a PCMCIA-specified credit-card-sized profile (54×85.6 mm), but exceed the Type III height of 10.5 mm.

The drive, which incorporates a PCMCIA-ATA interface, receives and sends data from its buffer at 4 Mbytes/sec; actual media transfers occur at rates from 1.4 to 2.8 Mbytes/sec. Typical seek time is 15 to 16 msec. The unit weighs 70g and withstands shocks of 30g (operating, no errors), 100g (operating with recoverable errors), and 300g (nonoperating). Power consumption ranges from 25 mW in sleep mode to 3W during spin-up. Evaluation samples are $499. Maxtor Corp, San Jose, CA, (408) 432-1700, FAX (408) 433-0457.

—by Gary Legg

# Team produces Unix pc-board design system

You can buy a complete Unix pc-board design system for £21,895 as a result of a teaming up of Racal-Redac and Sun Microsystems. The system comprises Racal-Redac's Visula Lite software (£15,000) and Sun Microsystem's SPARCstation LX hardware (£6895). The partners maintain that the system meets the demands of high-end PC-system users for more comprehensive networking, communications between tools, and high-performance autointeractive placement and routing.

Visula Lite is a reduced-function version of the company's high-end CAD Expert product. The package includes design capture, a pc-board layout editor, automatic placement and routing, library-management tools, and links through to manufacturing. The package is compatible with the company's other PC and workstation products, and there are trade-up incentives for PC users, along with migration tools for automatically transferring designs and libraries. Similar tools for PADS and PCAD users are planned.

The off-the-shelf software, on CD-ROM only, is available now from Racal-Redac's existing indirect distributors in Northern Europe. Worldwide distribution is planned for the second quarter of this year. Racal-Redac Systems Ltd, Tewkesbury, UK, (684) 294161, FAX (684) 299754; in the US, Westford, MA, (508) 692-4900, FAX (508) 692-4725. Sun Microsystems Ltd, Bagshot, UK, (276) 451440, FAX (276) 451287; in the US, Sun Microsystems Computer Corp, Mountain View, CA, (415) 960-1300, FAX (415) 969-9131.—by Brian Kerridge

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# Chip embodies programmable logic

The Flex 8000 chip family from Altera represents a new architectural approach to programmable logic that incorporates attractive features of both PLDs and field-programmable gate arrays (FPGAs). The chip's CMOS, static RAM-based design offers high register counts, predictable interconnect delays, low standby power, and in-circuit reprogramming. The basic logic element is a 4-input look-up table plus a register with a 5-nsec propagation delay. Each logic element also has inputs for creating wide cascaded functions and fast carry logic for adders and counters with 1-nsec propagation delay.

The architecture has only three interconnect-delay values: 1 nsec between the eight logic elements in the same logic array block, 6 nsec for logic elements in the same row, and 9 nsec across the chip. Maximum performance for a 16-bit up/down loadable counter is 70 MHz; max performance for a 24-bit adder is 50 MHz. The family will span 4000 to 24,000 gates. The 12,000-gate EPF81188 with 1008 logic elements, 180 I/O pins, and 1188 registers (in a 232-pin PGA) initially costs $495 (100); volume pricing for quad flatpacks drops to $198 (1000). Altera Corp, San Jose, CA, (408) 894-7000.—Doug Conner

# John Kemeny, Basic co-creator, dies

*John G Kemeny, co-creator of Basic, died December 26, 1992, at the age of 66. In 1964, Kemeny and his colleague Professor Thomas Kurtz created the Basic computer language, which remains a major teaching tool in computer programming.*

*Kemeny was born in Budapest, Hungary, and immigrated to the US in 1940. He graduated from Princeton University in 1947 and received his doctorate from Princeton in 1949 at the age of 23. As a student, Kemeny was a research assistant to Albert Einstein. He developed Basic at Dartmouth College, where he served as the school's 13th president from 1970 to 1981. Earlier in his career he took part in the Manhattan Project and in 1979, President Carter named him to head a 12-member commission to investigate the Three Mile Island nuclear-power-plant disaster.—by Susan Rose*

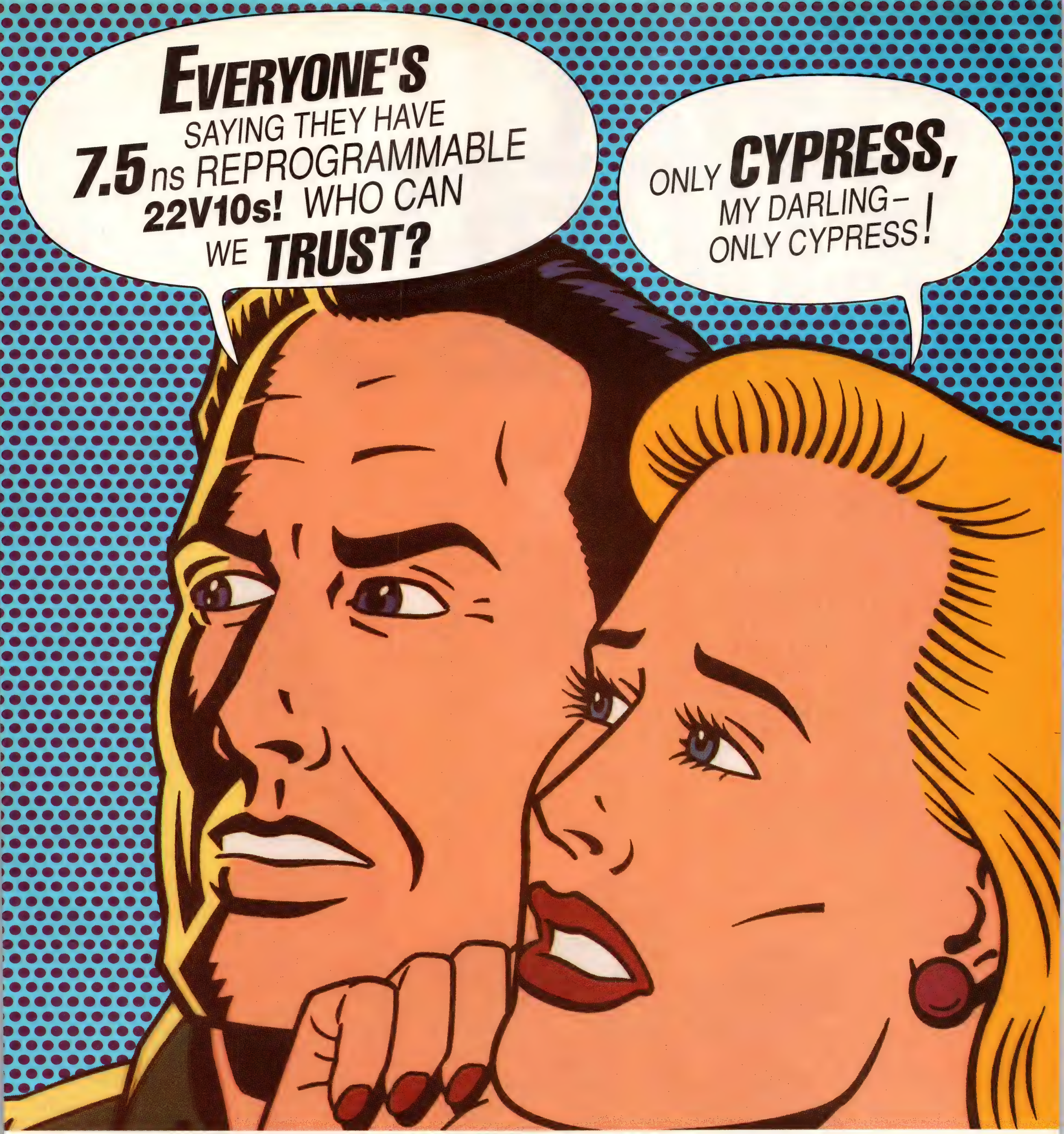
# Ethernet controller costs $15

The $15 (10,000) 82595 Ethernet controller from Intel integrates all major functions of a buffered LAN design (except buffer memory) into one chip. You can use up to 64 kbytes of dynamic RAM for local buffer memory and up to 256 kbytes of EEPROM or flash memory for booting operations. The chip interfaces directly to either an ISA or PCMCIA 2.0 bus and has power-management features for battery-powered applications. Packaged in a 144-lead TQFP (thin quad flatpack), the 1.7-mm-thick package fits PCMCIA I/O cards. Intel Corp, Santa Clara, CA, (800) 548-4725.—by Doug Conner

# Software tool simplifies logic selection

The Logic Integration Tool from Texas Instruments helps you select the appropriate logic implementation method for your design. Instead of researching vendor data sheets, you can use this tool to analyze the logic portion of your design for space, power, nonrecurring engineering, parts cost, and lead-time estimates. Select among standard TTL devices, PLDs, field-programmable gate arrays, and ASICs. The software runs on a PC and costs $59.95. Texas Instruments Inc, Dallas, TX, (800) 477-8924.

—by Doug Conner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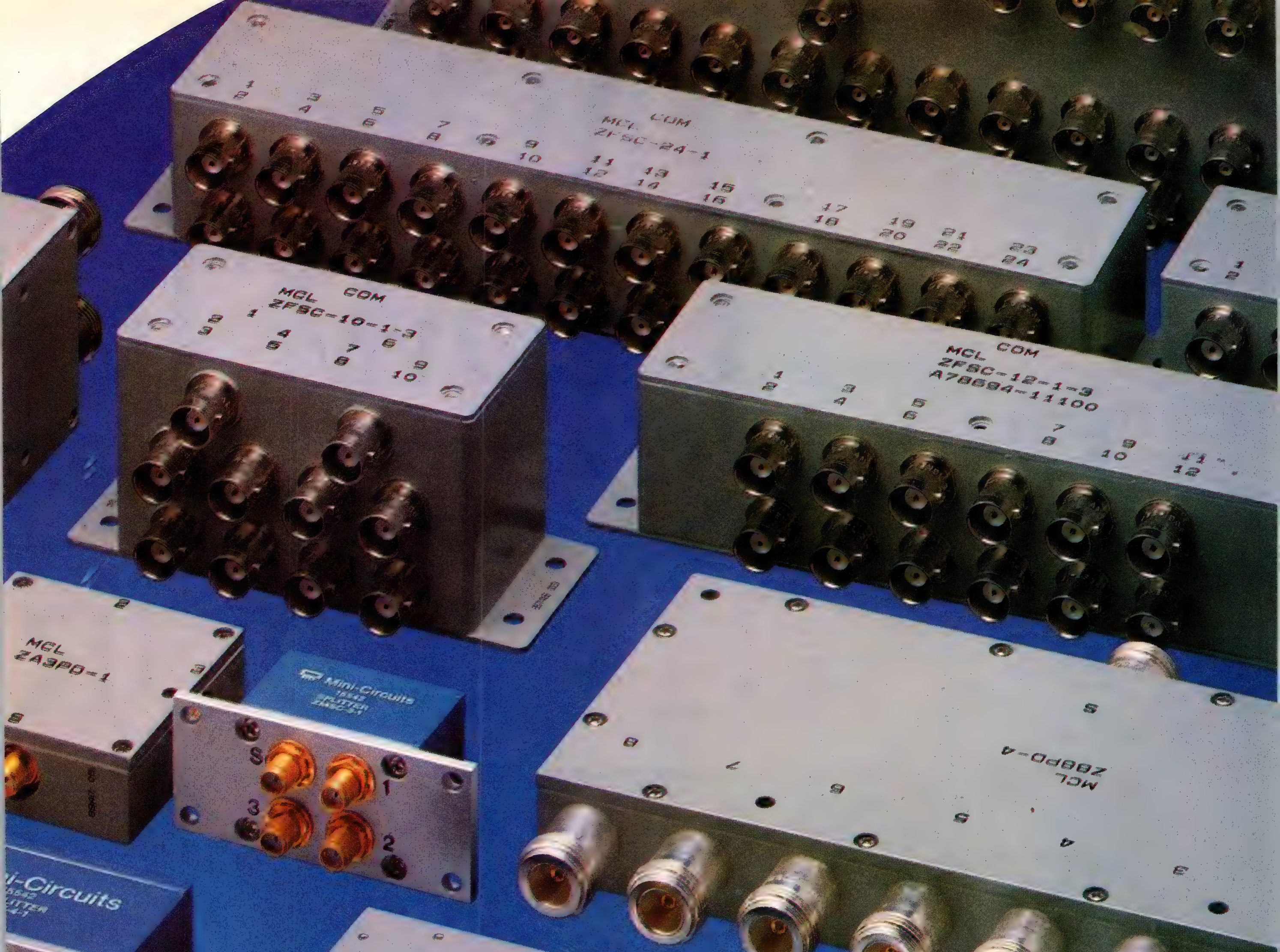

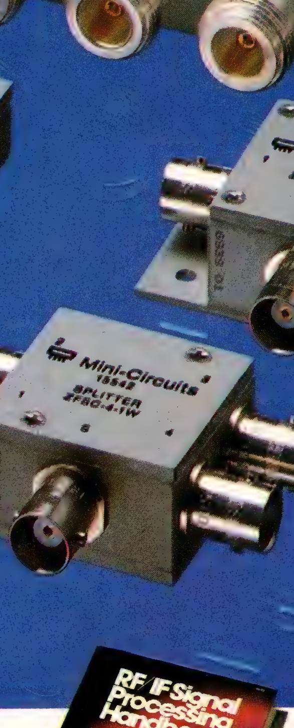

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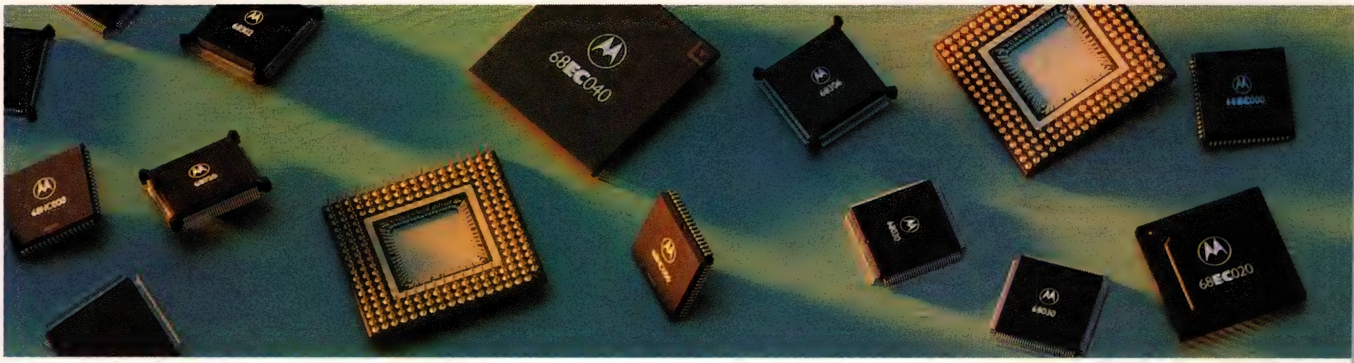

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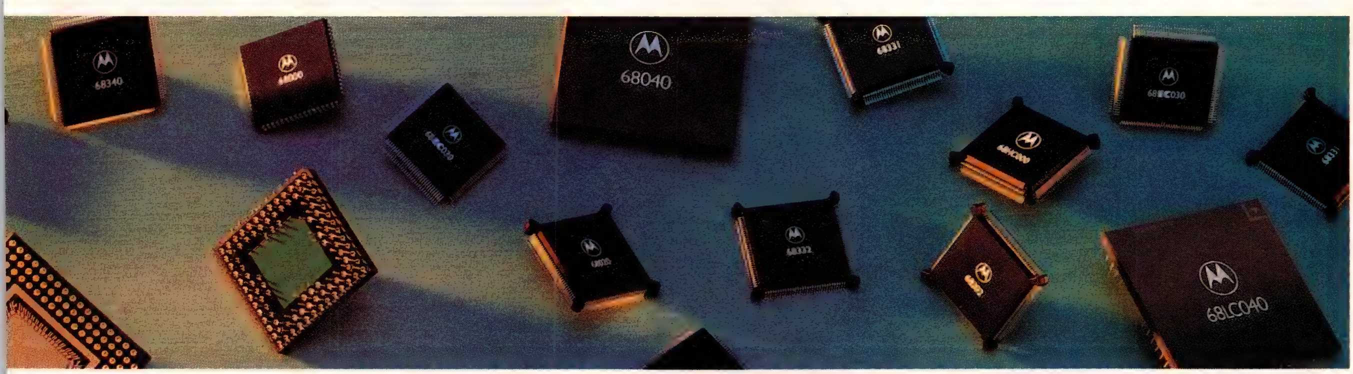

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CIRCLE NO. 26

# OrCAD Turns Another Page

OrCAD's Schematic Design Tools is the most popular electronic design automation product in the world. Designed by engineers for engineers, its "intelligent" interface and power features are a favorite for electronic designers in huge manufacturing companies and small job shops alike.

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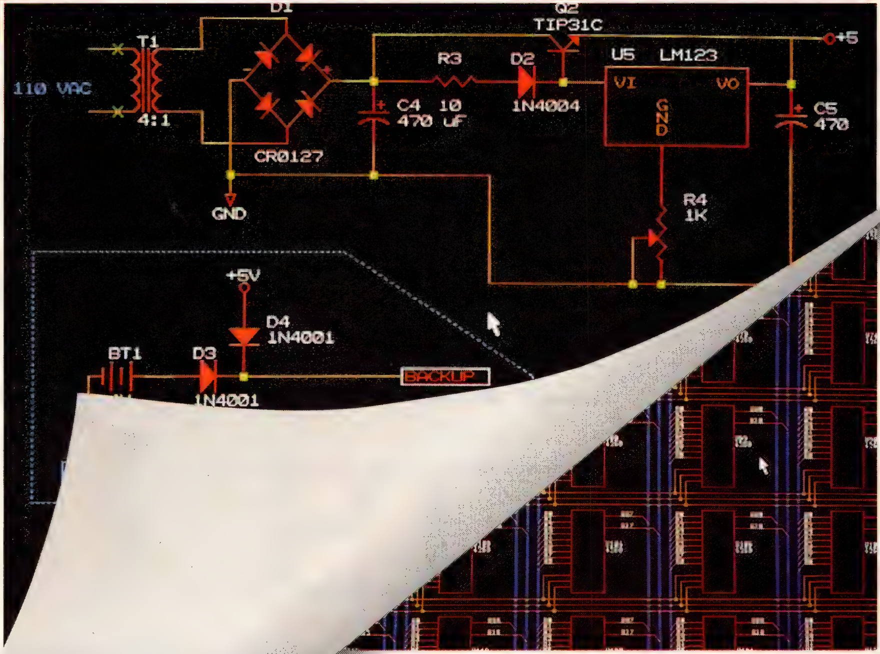

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CIRCLE NO. 27

## Reader expresses another view of cable TV

Jon Titus’ editorial, “Don’t tread on me” (EDN, April 9, 1992, pg 39), was on the mark until he went into the subject of cable TV. Although I don’t completely disagree with him, I think there is another view that the editorial side-steps:

- Cable isn’t available in many areas.
- Many people can’t afford cable even when it is available.
- The video (TV) medium is one of the easiest methods for conveying information to people worldwide. If it weren’t for the fact that a TV antenna attached to a TV is enough (most times) to pull in this information, many people would be forced to do without.

Without an informed electorate we suffer as a nation. I’m sure Titus will agree.

As for networks’ having a “stranglehold on our viewing habits,” it appears that their grip is getting ever tighter. Has Titus actually sat down and watched a network’s offerings over the course of a week? Most of the stuff (violence, stupid sitcoms, shock news) is utter garbage. For anyone with an education, most of this stuff is an intellectual insult.

For the most part, I follow Titus’s recommendation that ends the editorial—read a book or a magazine. This goes for my children as well.

*Michael Picco*
*Sierra Micro Research*
*Shingle Springs, CA*

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## Engineers cannot be all things to all problems

Jon Titus’ editorial, “Design product, not circuits” (EDN, July 20, 1992, pg 51), is of great concern to me as a systems engineer. Only the contributions of others in specific areas of design engineering make my job possible. Engineers cannot and should never try to be as Titus essentially suggests, “all things to all problems.” Effective management and coordination with individual areas of expertise and creativity make efficient solutions to problems possible. Reliance on “canned” solutions from others as some try to do only produces yesterday’s solutions and someone else’s idea of the correct way to achieve that solution.

The reference to the switch access problem is certainly not a new one, and the blame usually lies at the feet of a budget proposal or size constraint that was unrealistic in the first place. I haven’t met one person in 27 years in this business who would purposely design in a flaw as Titus describes.

Referring to the last paragraph of the editorial, any hardware designers who don’t understand the components they are using are doomed to misuse them. That is the one great failing of American engineering education these days: analog designers who don’t understand substrate interaction noise; RF designers who don’t understand the nonlinear effects of masking oxides; and digital designers who don’t understand intrinsic channel resistance change with temperature. We as producers of goods must keep a weather eye on the end result of our collective efforts, but antenna patterns are not the responsibility of the software department.

*Mark Hosford*
*Senior Systems Engineer*
*San Diego, CA*

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## Don’t forget MTOS

Oops, EDN inadvertently left out the address of Industrial Programming Inc in the October 15, 1992, issue Technical Update on embedded PCs (pg 67). IPI produces MTOS—a real-time multitasking, multiprocessing operating system for Intel and Motorola μPs.

Industrial Programming Inc
100 Jericho Quadrangle
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(516) 938-6600
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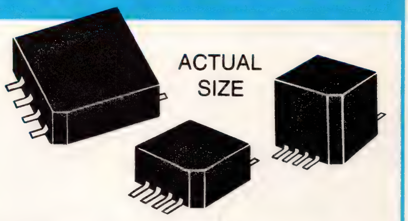
Transformers & Inductors



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CIRCLE NO. 28

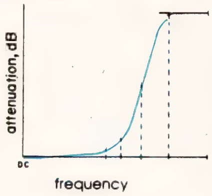
# FILTERS

# dc to 3GHz from $\$11^{45}$

## lowpass, highpass, bandpass

•less than 1dB insertion loss •greater than 40dB stopband rejection •surface-mount •BNC, Type N, SMA available •5-section, 30dB/octave rolloff •VSWR less than 1.7 (typ) •rugged hermetically-sealed pin models •constant phase •meets MIL-STD-202 tests •over 100 off-the-shelf models •immediate delivery

LOW PASS



## low pass, Plug-in, dc to 1200MHz

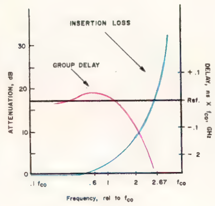
| Model No. | Passband MHz loss < 1dB | Stopband, MHz loss > 20dB | Stopband, MHz loss > 40dB | Model No. | Passband MHz loss < 1dB | Stopband, MHz loss > 20dB | Stopband, MHz loss > 40dB |
|---|---|---|---|---|---|---|---|
| ★LP-5 | DC-5 | 8-10 | 10-200 | ★LP-250 | DC-225 | 320-400 | 400-1200 |
| ★LP-10.7 | DC-11 | 19-24 | 24-200 | ★LP-300 | DC-270 | 410-550 | 550-1200 |
| ★LP-21.4 | DC-22 | 32-41 | 41-200 | ★LP-450 | DC-400 | 580-750 | 750-1800 |
| ★LP-30 | DC-32 | 47-61 | 61-200 | ★LP-550 | DC-520 | 750-920 | 920-2000 |
| ★LP-50 | DC-48 | 70-90 | 90-200 | ★LP-600 | DC-680 | 840-1120 | 1120-2000 |
| ★LP-70 | DC-60 | 90-117 | 117-300 | ★LP-750 | DC-700 | 1000-1300 | 1300-2000 |
| ★P-90 | DC-81 | 121-137 | 167-400 | ★LP-800 | DC-720 | 1080-1400 | 1400-2000 |
| ★LP-100 | DC-98 | 146-189 | 189-400 | ★LP-850 | DC-760 | 1100-1400 | 1400-2000 |
| ★LP-150 | DC-140 | 210-300 | 300-600 | ★LP-1000 | DC-900 | 1340-1750 | 1750-2000 |
| ★LP-200 | DC-190 | 290-390 | 390-800 | ★LP-1200 | DC-1000 | 1620-2100 | 2100-2500 |

Price, (1-9 qty), all models: plug-in $14.95, BNC $32.95, SMA $34.95, Type N $35.95

### Surface-mount, dc to 570MHz

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| SCLF-21.4 | DC-22 | 32-41 | 41-200 | SCLF-190 | DC-190 | 290-390 | 390-800 |
| SCLF-30 | DC-30 | 47-61 | 61-200 | SCLF-380 | DC-380 | 580-750 | 750-1800 |
| SCLF-45 | DC-45 | 70-90 | 90-200 | SCLF-420 | DC-420 | 750-920 | 920-2000 |
| SCLF-135 | DC-135 | 210-300 | 300-600 | | | | |

Price, (1-9 qty), all models: $11.45

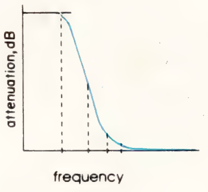


### Flat Time Delay, dc to 1870MHz

| Model No. | Passband MHz loss < 1.2dB | Stopband MHz loss > 10dB | Stopband MHz loss > 20dB | VSWR Freq. Range, DC thru 0.2fco X̄ | VSWR Freq. Range, DC thru 0.6fco X̄ | Group Delay Variations, ns Freq. Range, DC thru fco X̄ | Group Delay Variations, ns Freq. Range, DC thru 2fco X̄ | Group Delay Variations, ns Freq. Range, DC thru 2.67fco X̄ |
|---|---|---|---|---|---|---|---|---|
| ★BLP-39 | DC-23 | 78-117 | 117 | 1.3:1 | 2.3:1 | 0.7 | 4.0 | 5.0 |
| ★BLP-117 | DC-65 | 234-312 | 312 | 1.3:1 | 2.4:1 | 0.35 | 1.4 | 1.9 |
| ★BLP-156 | DC-94 | 312-416 | 416 | 0.3:1 | 1.1:1 | 0.3 | 1.1 | 1.5 |
| ★BLP-200 | DC-120 | 400-534 | 534 | 1.6:1 | 1.9:1 | 0.4 | 1.3 | 1.6 |
| ★BLP-300 | DC-180 | 600-801 | 801 | 1.25:1 | 2.2:1 | 0.2 | 0.6 | 0.8 |
| ★BLP-467 | DC-280 | 934-1246 | 1246 | 1.25:1 | 2.2:1 | 0.15 | 0.4 | 0.55 |
| ▲BLP-933 | DC-560 | 1866-2490 | 2490 | 1.3:1 | 2.2:1 | 0.09 | 0.2 | 0.28 |
| ▲BLP-1870 | DC-850 | 3740-6000 | 5000 | 1.45:1 | 2.9:1 | 0.05 | 0.1 | 0.15 |

Price, (1-9 qty), all models: plug-in $19.95, BNC $36.95, SMA $38.95, Type N $39.95
NOTE: ▲: -933 and -1870 only with connectors, at additional $2 above other connector models.

HIGH PASS

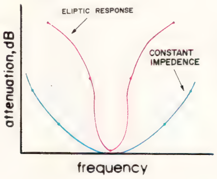


## high pass, Plug-in, 27.5 to 2200MHz

| Model No. | Stopband MHz loss < 40dB | Stopband MHz loss < 20dB | Passband, MHz loss < 1dB | VSWR Pass-band Typ. | Model No. | Stopband MHz loss < 40dB | Stopband MHz loss < 20dB | Passband, MHz loss < 1dB | VSWR Pass-band Typ. |
|---|---|---|---|---|---|---|---|---|---|
| ★HP-25 | DC-13 | 13-19 | 27.5-200 | 1.8:1 | ★HP-400 | DC-210 | 210-290 | 395-1600 | 1.7:1 |
| ★HP-50 | DC-20 | 20-26 | 41-200 | 1.5:1 | ★HP-500 | DC-280 | 280-365 | 500-1600 | 1.8:1 |
| ★HP-100 | DC-40 | 40-55 | 90-400 | 1.8:1 | ★HP-600 | DC-350 | 350-440 | 600-1600 | 2.0:1 |
| ★HP-150 | DC-70 | 70-95 | 133-600 | 1.8:1 | ★HP-700 | DC-400 | 400-520 | 700-1800 | 1.6:1 |
| ★HP-175 | DC-70 | 70-105 | 160-800 | 1.5:1 | ★HP-800 | DC-445 | 445-570 | 780-2000 | 2.1:1 |
| ★HP-200 | DC-90 | 90-116 | 185-800 | 1.6:1 | ★HP-900 | DC-520 | 520-660 | 910-2100 | 1.8:1 |
| ★HP-250 | DC-100 | 100-150 | 225-1200 | 1.3:1 | ★HP-1000 | DC-550 | 550-720 | 1000-2200 | 1.9:1 |
| ★HP-300 | DC-145 | 145-170 | 290-1200 | 1.7:1 | | | | | |

Price, (1-9 qty), all models: plug-in $14.95, BNC $36.95, SMA $38.95, Type N $39.95

BANDPASS



## bandpass, Elliptic Response, 10.7 to 70MHz

| Model No. | Center Freq. (MHz) | Passband I.L. 1.5 dB Max. (MHz) | 3 dB Bandwidth Typ. (MHz) | Stopbands I.L. > 20dB at MHz | Stopbands I.L. > 35dB at MHz |
|---|---|---|---|---|---|
| ★BP-10.7 | 10.7 | 9.6-11.5 | 8.9-12.7 | 7.5 & 15 | 0.6 & 50-1000 |
| ★BP-21.4 | 21.4 | 19.2-23.6 | 17.9-25.3 | 15.5 & 29 | 3.0 & 80-1000 |
| ★BP-30 | 30.0 | 27.0-33.0 | 25-35 | 22 & 40 | 3.2 & 99-1000 |
| ★BP-60 | 60.0 | 55.0-67.0 | 49.5-70.5 | 44 & 79 | 4.6 & 190-1000 |
| ★BP-70 | 70.0 | 63.0-77.0 | 68.0-82.0 | 51 & 94 | 6.0 & 193-1000 |

Price, (1-9 qty), all models: plug-in $18.95,
BNC $40.95, SMA $42.95, Type N $43.95

### Constant Impedance, 21.4 to 70MHz

| Model No. | Center Freq. MHz | Passband MHz loss < 1dB | Stopband loss > 20dB at MHz | VSWR 1.3:1 Total Band MHz |
|---|---|---|---|---|
| ★IF-21.4 | 21.4 | 18-25 | 1.3 & 150 | DC-220 |
| ★IF-30 | 30 | 25-35 | 1.9 & 210 | DC-330 |
| ★IF-40 | 42 | 35-49 | 2.6 & 300 | DC-400 |
| ★IF-50 | 50 | 41-58 | 3.1 & 350 | DC-440 |
| ★IF-60 | 60 | 50-70 | 3.8 & 400 | DC-500 |
| ★IF-70 | 70 | 58-82 | 4.4 & 490 | DC-550 |

Price, (1-9 qty), all models: plug-in $14.95,
BNC $36.95, SMA $38.95, Type N $39.95

NOTE: ★**Add Prefix P, B, N, or S for Pin, BNC, N, or SMA connector requirement.**

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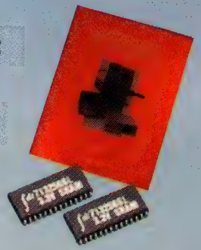

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# ASK EDN

EDITED BY JULIE ANNE SCHOFIELD

## Sorry, wrong number

In the November 12, 1992, Ask EDN, reader Manuel Vaz Guedes wrote that he wanted to download some fuzzy-logic freeware from the Motorola computer bulletin-board system (BBS). The number in the reply is wrong. Ask EDN regrets the error.

First of all, Motorola has several bulletin boards. The BBS with the fuzzy-logic software is the MCU BBS. Its number is (512) 891-3733; 300 to 9600 baud; 8,N,1. The sysop is John Dumas, who reports that the user interface is not difficult to use and now includes a FAX server called FreeFAX. This server lets callers select and receive FAX documents including fuzzy-logic application notes.

## References hard to find in Croatia

**I have read your advertisements about many good technical books that cover electronics and computers. As I am a student programmer, I am interested in programming the 8051 microcontroller, especially the SAB 80537 version.**

**Could you recommend any good books or other sources that cover 8051 programming? There is never enough knowledge, and here in Croatia it is much easier to buy hardware than find good technical references or specialized software.**

***Damir Marasovic***
***Zagreb, Croatia***

Technical Editor Ray Weiss responds: The 8-bit 8051 is a good microcontroller (μC) for you to be working with. Its architecture is a bit baroque, but many engineers characterize it as the Model T (as in the early popular Ford car) of μCs because of its popularity, wide range of clock speeds and peripheral mixes, and large base of development tools.

A good book about the processor is *The 8051 Microcontroller—Architecture, Programming, and Applications* by Kenneth J Ayala, 1992 (West Publishing Co, 50 W Kellog Blvd, St Paul, MN 55164. Phone (612) 687-7000.). The text comes with an assembler, simulator, and workbook with complete project code. It also includes 8051 design projects to build your design skills.

A couple of new books I'm looking at are *C and the 8051—Programming and Multitasking* by Thomas W Schultz, 1992 (Prentice-Hall, Route 9W, Englewood Cliffs, NJ 07632. Phone (201) 592-2000) and *The 8051 Microcontroller*, by F Scott MacKenzie, 1992 (Macmillan Publishing Co Inc, 866 Third Ave, New York, NY 10022. Phone (212) 702-2000.).

## Contact needs supervision

**I'm looking for a circuit that will electrically supervise either a normally open or a normally closed contact. My application is to be used in a communications/signaling system. By electrically supervise, I mean that the circuit must be able to detect a single open, a single ground, or a short of two or more conductors extending to the pc board that contains the supervised contact. The supervision circuit does not need to distinguish between these three failure modes, and it does not need to detect a fault condition that would still allow the change of state of the contact to be detected. It would also be very nice if multiple contacts could be wired in parallel if normally open contacts are used or in series if normally closed contacts are used.**

**My research and design efforts have developed only a voltage window detector that has two separate windows of safe operation. If the sensing conductor is in the first window, the contact is open. If the sensing conductor is in the second window, the contact is closed. If the sensing conductor is outside the two windows, there's a fault in the system. I'm not excited about this design approach and am looking for a better technique.**

**An approach that is commonly used but is too expensive for my application is putting a microcontroller on the pc board containing the contact to be supervised. The controller would then communicate over a serial link, which would be supervised by a polling process. Any other suggestions would be appreciated.**

***Curt Geiger***
***Hill-Rom***
***Batesville, IN***

We forwarded your question to Bob Pease at National Semiconductor Corp (Santa Clara, CA): First of all, this is a SYSTEM PROBLEM, and there are no simple solutions that don't affect lots of things. IF, for example, the contacts are right at GROUND, and if you already have a power supply such as 5V, then that's pretty easy. You can feed it 1 μA from a 4.7-MΩ resistor and see if the contact is open or closed or somewhere in the middle. But if you want to be able to detect ANY contacts, anywhere in space, serial or parallel, then the problem is so vague that there's no rational solution. If you can narrow it down somewhat, that may suggest five possible solutions. THEN if you can say what's wrong with each of those solutions, you'd have a chance to design a system that would probably work ok.

Or if you could define a system that does some of the things you like but is deficient in two or three aspects, that would help things a lot, too.

## NeoCAD, where are you?

**In the October 22, 1992, issue of EDN Products & Careers, I read an article about the company NeoCAD. Do you have a phone number for the company?**

***Bob Colburn***
***Pensar Corp***
***Appleton, WI***

The company information is

NeoCAD
2585 Central Ave
Boulder, CO 80301
(303) 442-9121
FAX (303) 442-9124.

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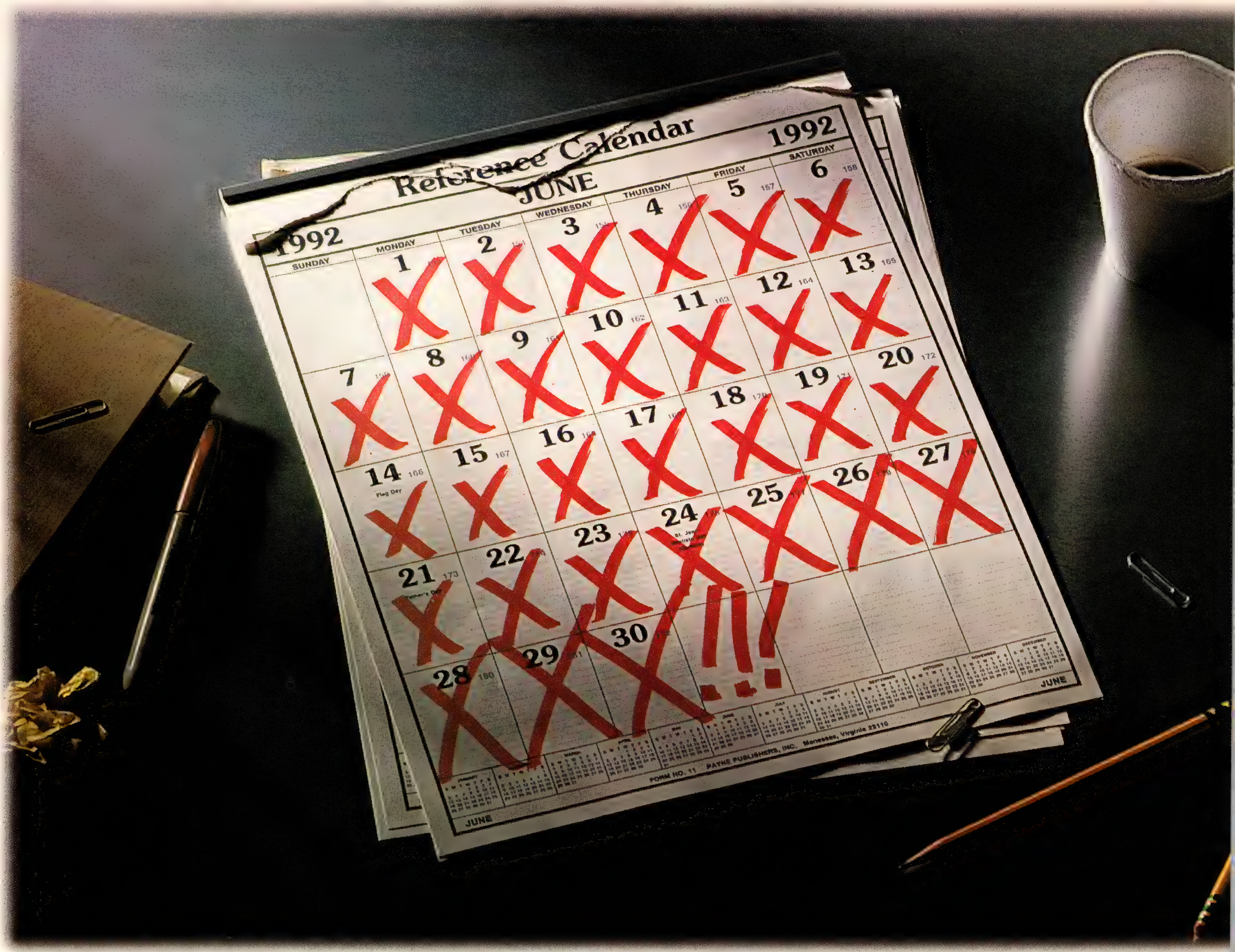

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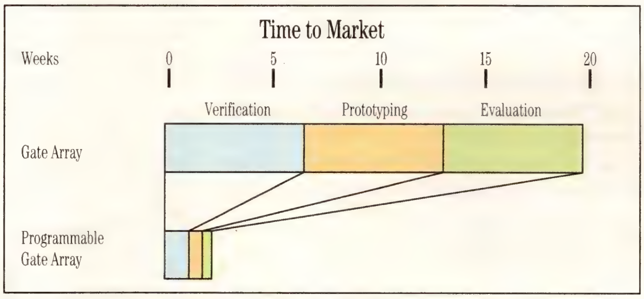

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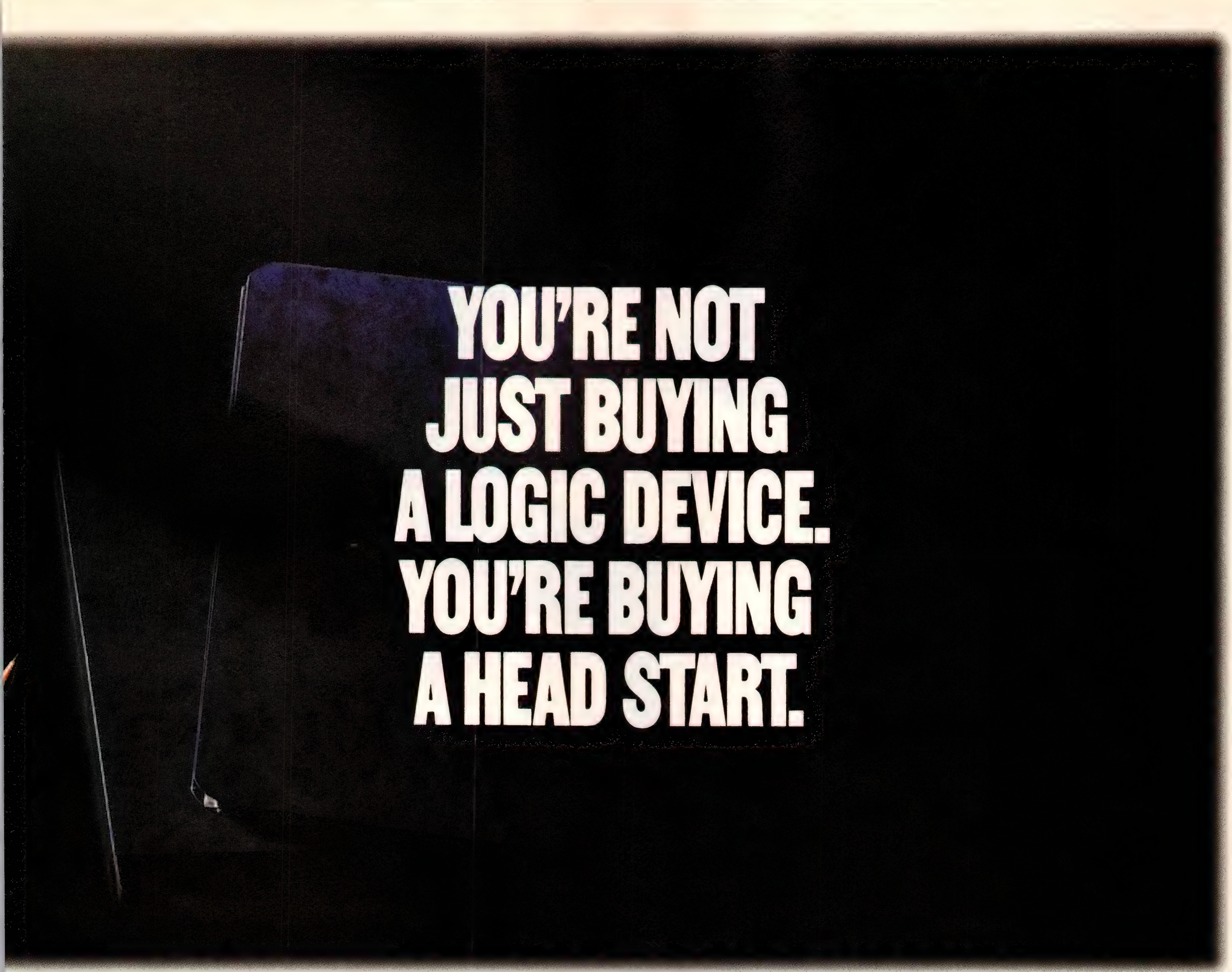

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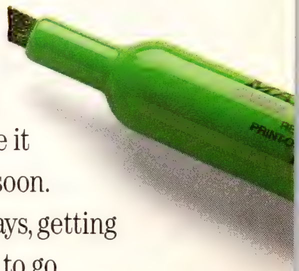

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CIRCLE NO. 31

# What's the simplest way to generate a mid-rail ground in a single-supply system?

# TI's industry-first TLE2425/6 Virtual Ground Generators.

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They can source or sink 20 mA while maintaining a load regulation of 150 µV (typ). In a single-supply, 5-V system, the TLE2425 outputs an ultrastable 2.5 V; the TLE2426 "Rail Splitter" divides any supply, 4 V to 40 V, in half.

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**TLE2425/6 Overview**

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- Space-saving TO-92 or SO-8 packages
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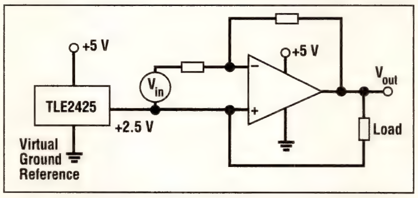

***TI's virtual ground generator** provides stable reference for single-supply systems.*

## For a free sample pack

and more information on the TLE2425/6, please circle the number given below on the reader service card.

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CIRCLE NO. 83

# Curse of the shrunken head

My brother Chris wasn't particularly superstitious, but he didn't like to go close to my grandfather's barn. If Mom or Dad asked him to go over and lock up the barn or get firewood out of it, he'd balk. Frankly, all of us kids thought the barn was a bit spooky, particularly at night, but it was a great place to play. One day when we were a bit older, we asked Chris why he didn't like the barn. He said it was because of the shrunken head. "Shrunken head!" we exclaimed, "What shrunken head?" "There's a shrunken head hanging in there and it's scary," he said.

We weren't sure whether or not to take a look, but we screwed up our courage and peeked in. Sure enough, there was a shrunken head hanging up in the far corner of the barn where it was dark and out of the way. We'd missed seeing it all these years. When we asked our grandfather about the grizzly remains of a headhunter's ritual, all he could say was, "What are you kids talking about? There's no shrunken head in the barn." We insisted there was, so we decided on an expedition—in the company of an adult and in daylight—to find the truth.

"That's just an old ball of twine that got put up there when we were wrapping plants," said Grandpa. "That was years ago. Looks like birds just pulled it to pieces for nesting materials. It looks a bit like a shrunken head, though, particularly if you're a kid."

When we look at our fears in the light of day and in the context of everything else we have to do, some of them seem less fearsome. This isn't meant to belittle fears that are real—the fear of having an operation, of facing a job layoff, or of losing a loved one. Yet, many of us go through life being worried about things that we can either change, or that don't seem so fearful on closer examination. If I wake up at night and toss and turn, thinking about things facing me at work or at home, I usually get up, write them down, and go back to sleep. After eating a good breakfast, the list doesn't seem so terrible. Some people go for a walk, or work in their garden as ways of putting fears in proper perspective. Putting fears in perspective often diminishes them.

By the way, when Grandpa retired from the nursery business, we turned the barn into a clubhouse. Newcomers had to climb up and touch the shrunken head before they could join the club. Those who wouldn't touch it—and never discovered it was just twine—had to live with the curse forever. Life's like that.

Jon Titus

**Jon Titus**
**Editor**

**Jesse H. Neal**
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1990 Certificate, Best Series
1987, 1981 (2), 1978 (2),
1977, 1976, 1975

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1991, 1990, 1988, 1983, 1981

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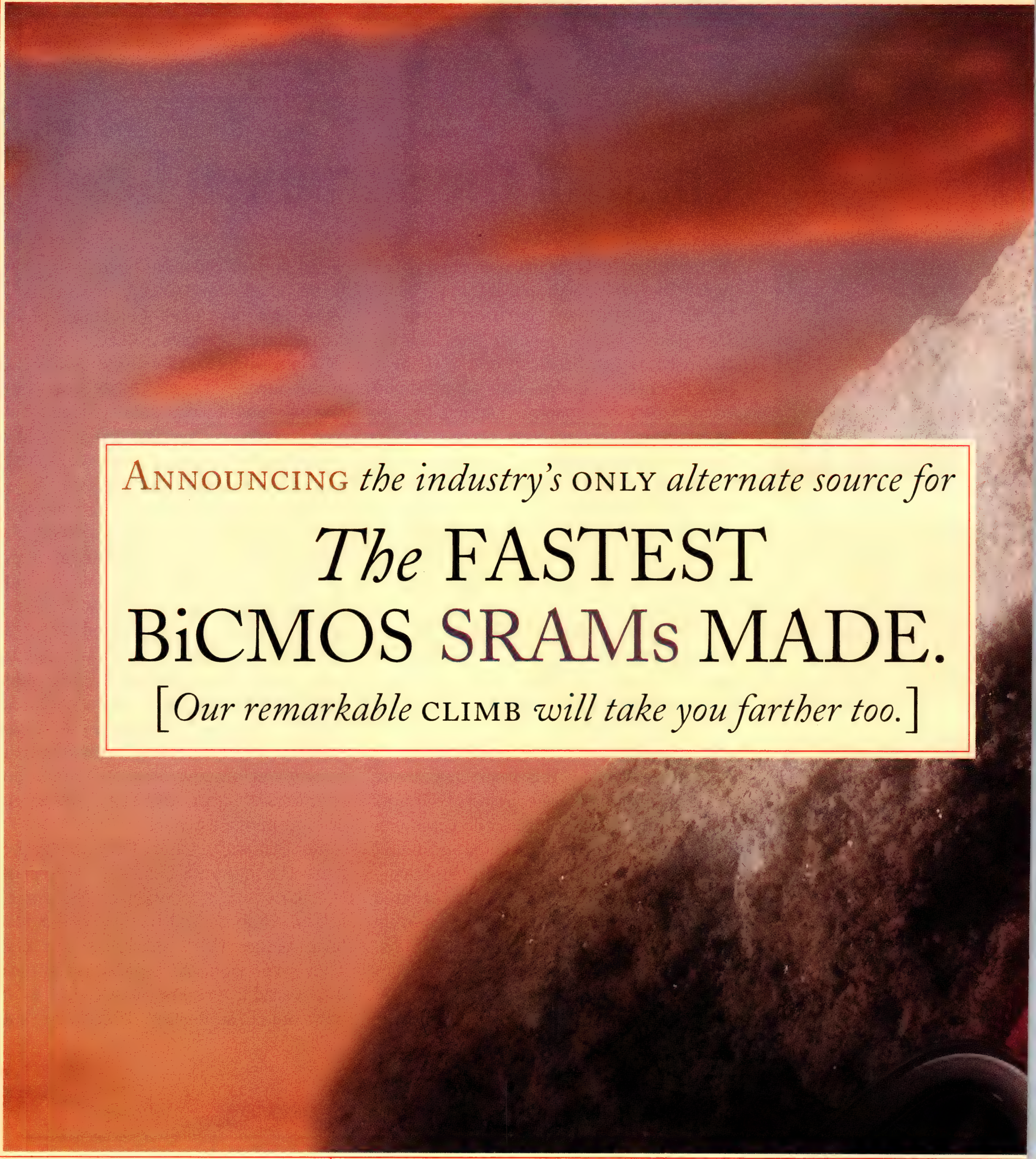

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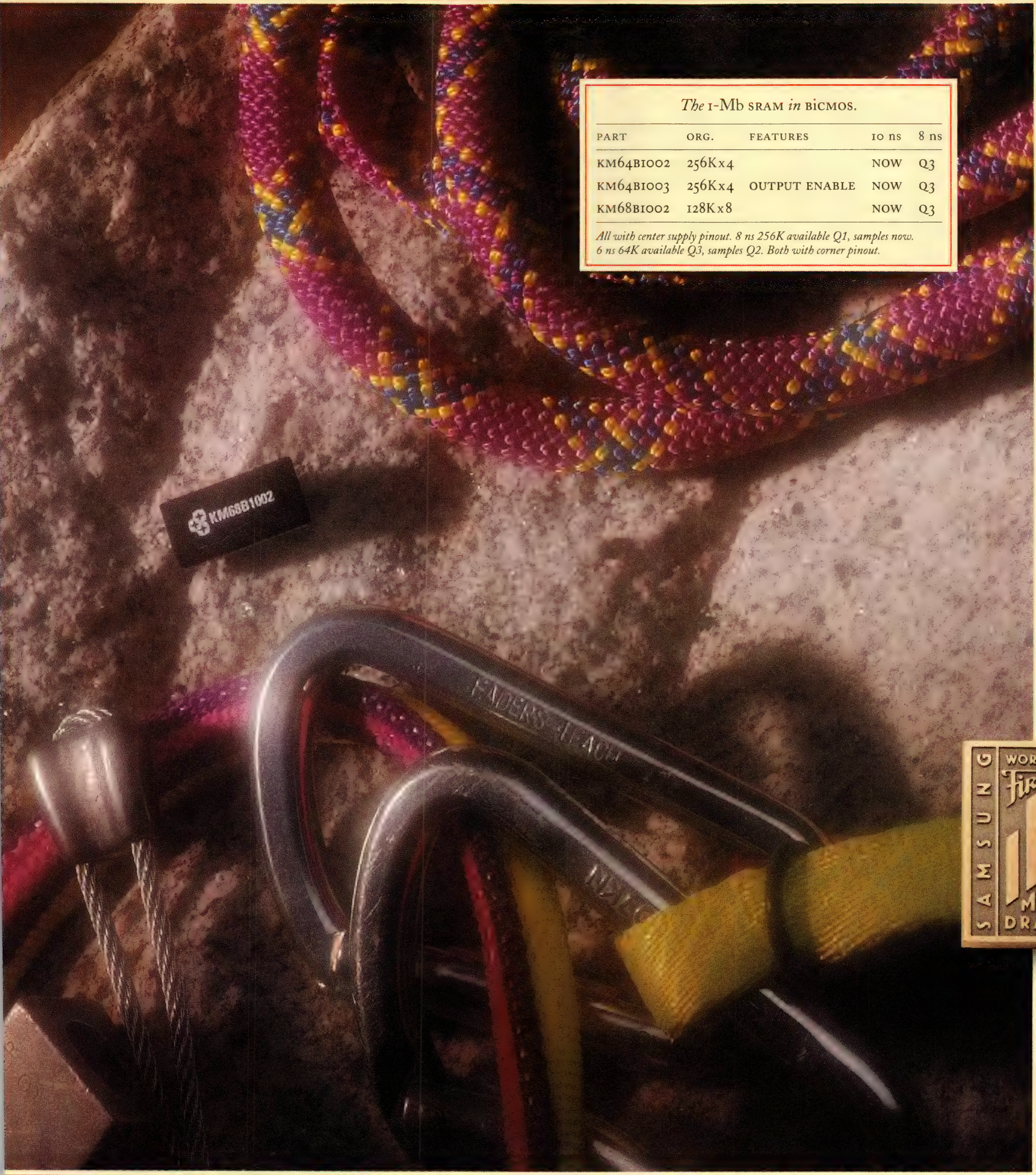

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*All with center supply pinout. 8 ns 256K available Q1, samples now. 6 ns 64K available Q3, samples Q2. Both with corner pinout.*

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CIRCLE NO. 34

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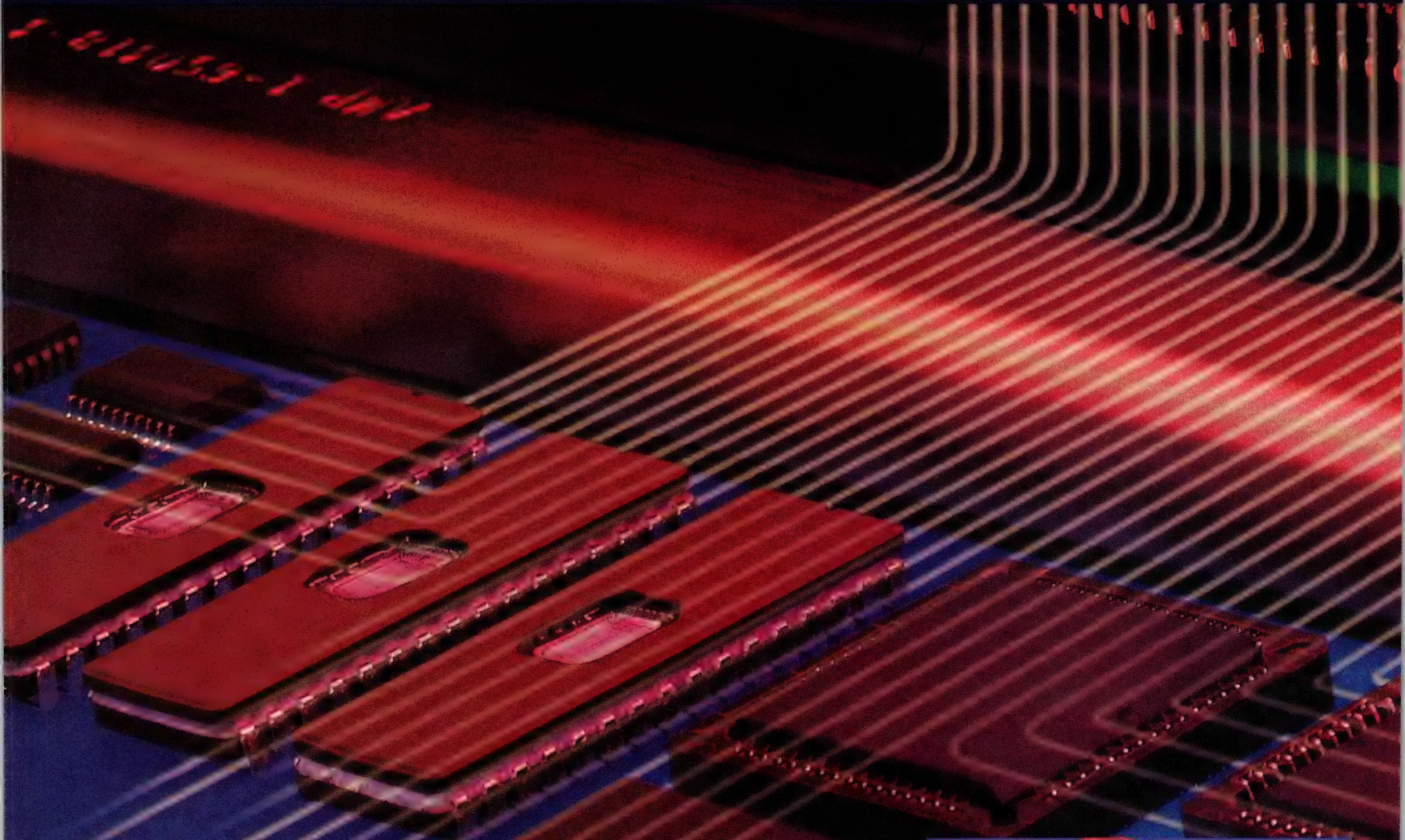
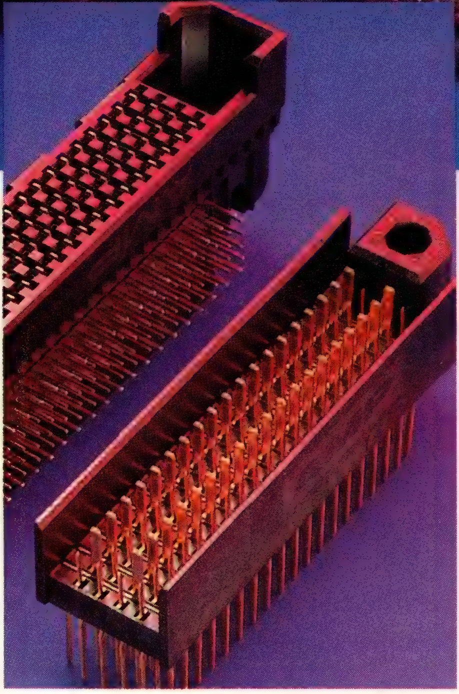


# THIS IS AMP TODAY.



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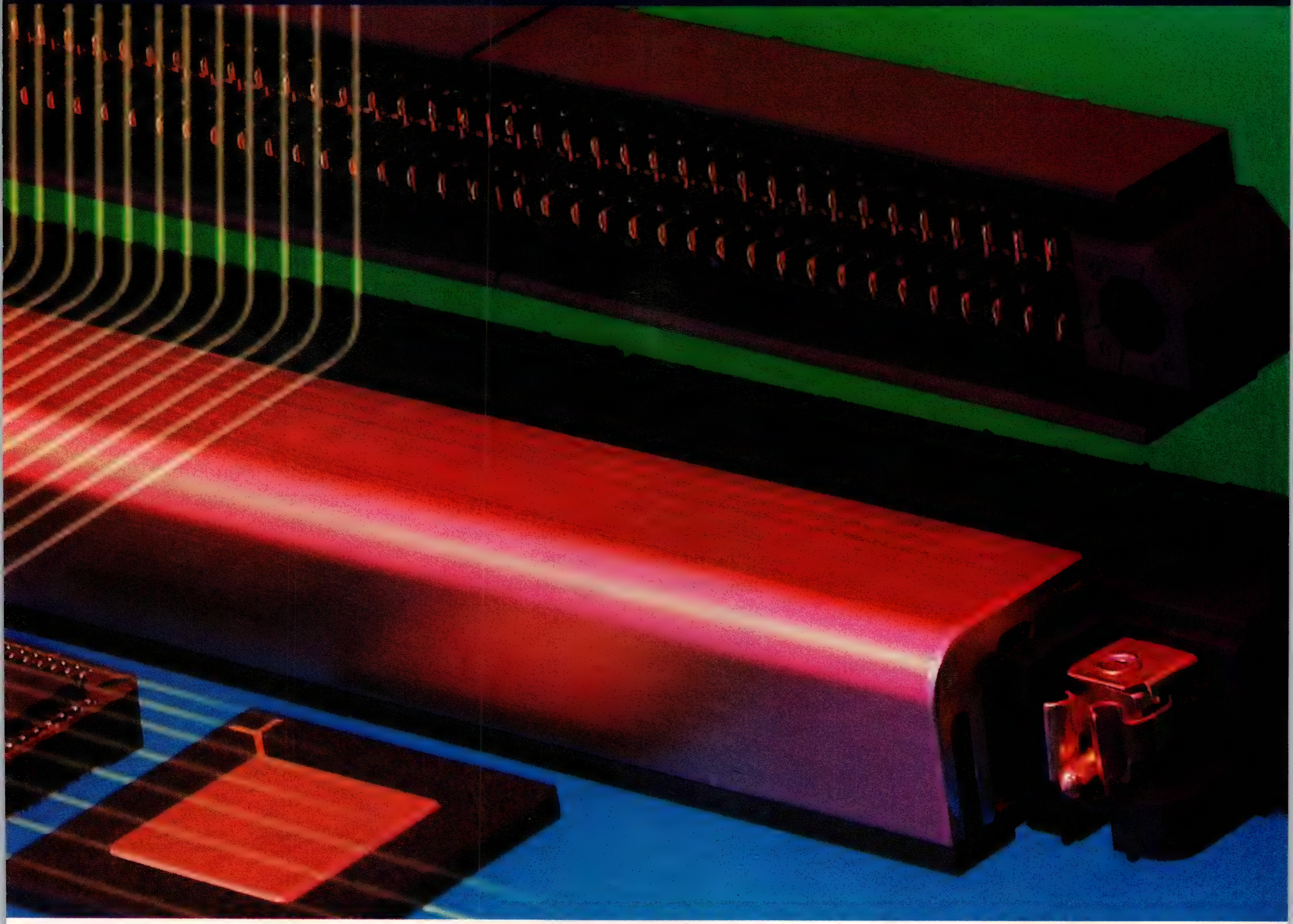

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Our modular, scalable Stripline 100 connector system can accommodate edge rates of 250 ps (500 ps at <3% crosstalk), and still give you 40 signal lines per inch – all four rows on a .1"x.1" grid. Reference planes isolate individual signal columns within the standard grid geometry, creating an interface completely transparent to high-speed logic.

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CIRCLE NO. 35

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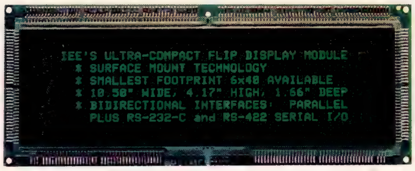
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* BIDIRECTIONAL INTERFACES: PARALLEL
PLUS RS-232-C and RS-422 SERIAL I/O

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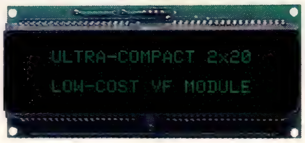
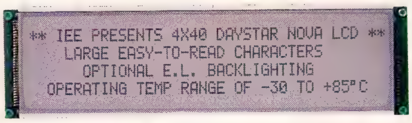
IN SMT PACKAGE, 7.85"W x 2.03"H x .94"D



- The **"NO-FRILLS"™** and **"NINETY SERIES"™** are IEE's **low-cost VFDs** with a high-priced appearance and are ideal for OEM applications such as copiers, POS terminals, pay telephones, etc.
- **"Industrial Strength" FLIPs** feature 9, 11, and 15mm characters, making them easy to read from longer distances—typical on factory floors and in PLC applications.

### Liquid Crystal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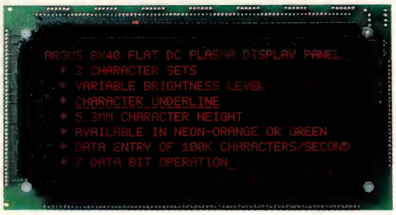
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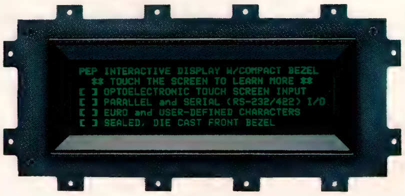
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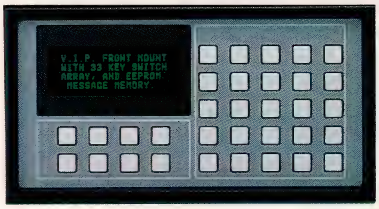

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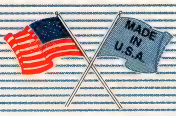

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Immediate Circle #36

Reference Circle #37

# External power supplies enhance system design options

**TOM ORMOND,** Senior Technical Editor

**External power supplies are no longer looked upon as low-cost, technically inferior products designed solely for consumer goods. Today, they are being accepted as the primary power source for a variety of advanced products.**

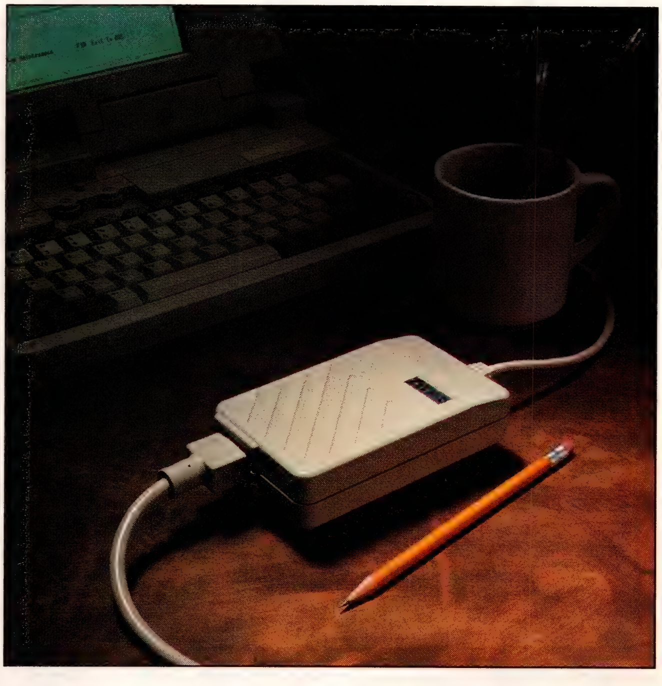
External power supplies offer the designer the most comprehensive array of power-supply parameters available for small-package applications. As a result, they have become an accepted mode of power in many applications today. System specifiers can use the units to simplify the physical design and packaging of their products, enhance the aesthetics of the product, and reduce product development and assembly costs.

A number of factors are spurring the interest in the use of external power supplies. For one thing, the market segments where external power supplies are particularly well suited—portable and hand-held equipment—are expanding. The demand for smaller and lighter products continues unabated, and the easiest way for many OEMs to meet these demands is to remove the supply from their product enclosure. Getting rid of the internal supply does more than save space and weight—it removes a source of hazardous voltage, heat, and magnetic interference from the enclosure. The heat consideration can be crucial as system product designers strive to decrease the size of their products.

Secondly, when OEMs remove the supply from the enclosure they no longer have to worry about meeting various agency safety standards for the supply—it's no longer an integral part of the product.

Customer convenience is another point to consider when it comes to external versus internal power sources. In an electronic product, a failure in the power-supply module is certainly not uncommon. With an internal power supply, the customer must arrange for product repair, which is costly and time-consuming for the customer or the product manufacturer, if the unit is still under warranty. Using an external power supply eliminates such inconveniences. In the event of a failure, the customer simply replaces the supply—no special expertise is needed. The bottom line is savings in time and money.

Another driving force is flexibility. The use of external rather than internal supplies simplifies the OEM's task when



**MIADA Series supplies from Elpac are housed in a 3x5x2.3-in. molded case. The line includes 26 models with single outputs between 12 and 24V and power levels as high as 28W.**

dealing in the international marketplace. Vendors can offer the same product for both domestic and foreign markets without having to worry about power-line differences.

One final point to consider is cost. In many cases, manufacturers of external power supplies can deliver a stand-alone power source for less than an OEM can build a supply into his product.

### So what's an external supply?

Outside of output-power capabilities, there aren't many differences between external and internal power supplies. External power supplies use the same sort of components found in internal supplies—advanced power MOSFETs and surface-mount components—to pack more power into smaller packages.

External power supplies are available in linear or switching types. The devices are available in two configurations. In one, the ac plug is built right into the case of the supply so that the plug prongs physically attach the case to the wall outlet. The second style has a length of ac cord running from the wall plug to the power supply case that sits on a table or desktop.

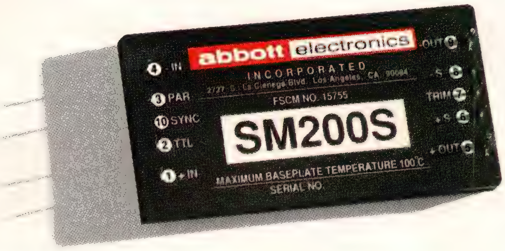
**A universal input of 90 to 264V ac is a key feature of the SW Series 48W, single-output supplies from Ault. Housed in a 94V-0-rated polycarbonate enclosure, the devices are IEC, TUV, UL, and CSA approved and meet VDE and FCC Class B emission standards.**

Given the performance parameters listed in **Table 1**, system circuitry would find it hard to determine whether the power source is internal or external. Now, external supplies are available in single-, dual-, and triple-output versions. Output voltages cover all the bases ranging from 5 to 48V, and power levels are available to handle just about any moderate-size application. One feature that is also standard in today's external power supplies is universal input. The majority of the units listed in **Table 1** operate from voltages of 85 to 264V ac without having to use jumpers or switches to convert the input from 115 to 230V operation. The supplies internally adjust to the input voltage automatically.

Today's external power supplies have some other noteworthy characteristics that are not shown in **Table 1**. Efficiency figures, for example, exceed 80% in many cases, and output-voltage accuracies of 1% are available. External supplies also offer a good deal of protection features as standard. Practically all units include overcurrent and overvoltage protection; some supplies even offer overtemperature (with automatic reset) protection as standard. MTBF figures of 100,000 hours are not uncommon, and some of the supplies have shown MTBF figures approaching 1 million hours.

**Table 1—Representative external supply parameters**

| Manufacturer | Model | Type | Input voltages (V ac) | Output power (W) | Number of outputs | Output voltages (V dc) | Size (in.) | Approvals | Price |
|---|---|---|---|---|---|---|---|---|---|
| **Ault Inc** | SW Series | Desktop | 100 to 250 | 17 to 48 | 1, 3 | 5, 12, −12, 15, −15, 24 | 5.87×3.4×2.0 | UL, IEC, TUV, CSA, FCC | $48 (500) |
| **Autec Power Systems** | UPS20P | Desktop | 85 to 264 | 20 | 1, 2 | 5, 9, 12, 15, 24 | 5.83×2.95×1.83 | FCC, UL, CSA, TUV, VDE | $33.17 (1000) |
| **CUI Stack** | DPR Series | Wall mount | 175, 230 | 1.8 to 18 | 1, 3 | 5, 9, 12, 18, 32 | 2.0×2.0×1.5 | UL, CSA | $3 to $20 (OEM qty) |
| **Custom Power Systems** | CPS 1121 | Wall mount | 90 to 135 | 112 | 1 | 28 | 3.0×5.5×2.0 | UL pending | $125 (1000) |
| **Elpac Power Systems** | MIADA | Desktop | 90 to 264 | 20 to 28 | 1 | 12 through 24 in 1V increments | 3.0×5.0×1.3 | UL, CSA, TUV | $35 |
| **International Power Sources** | PUP 55 | Desktop | 85 to 264 | 55 | 1, 2, 3 | 5, 12, −12, 15, −15, 24, 36 | 6.97×3.74×2.25 | UL, CSA, IEC | $40 |
| **James Electronics** | 13000 Series | Desktop | 120 | 10 to 50 | 1 | 8, 12, 16, 20, 28, 34, 48 | 4.74×3.05×2.2 | UL, CSA, FC | $10 to $24 (OEM qty) |
| **LZR Electronics** | LZUS 2500 Series | Desktop | 90 to 265 | 25 | 1, 2, 3 | 5, 9, 12, 15, 18, 24 | 4.3×2.7×1.45 | UL, CSA, TUV, FCC, VDE | $35 (1000) |
| **Tamura Corp** | SWA | Desktop, wall mount | 90 to 264,<br>90 to 132,<br>198 to 264 | 15 to 60 | 1 | 5 to 17.5 | 7.87×3.94×2.6 | UL, CSA, VDE | From $39 |



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- Highest density in the solar system
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- Power limit: undetermined
- Variable frequency; derating nonverifiable
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- Extended input voltage range: 1-$10^{43}$Vdc
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- Mil-Std qualifications: none
- Board-mountable: *not*
- Readily available; not deliverable in unit form
- Price: *very* expensive

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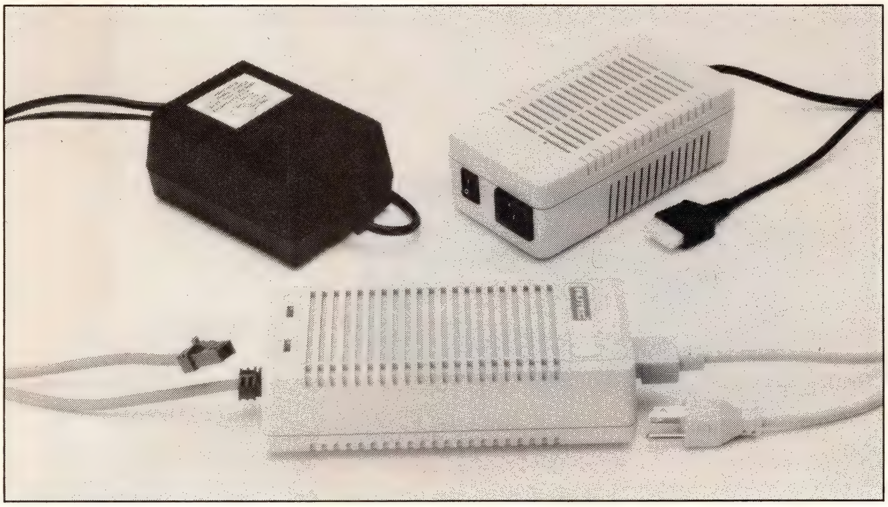

**Autec's UPS20P Series 20W supplies are available in both single- and dual-output versions. A universal input ensures compatibility with any power mains throughout the world.**

The enclosures used in today's external supplies actually enhance supply reliability. With the supply sitting out in the open, the enclosure must be able to handle impacts and maintain structural integrity. Many of the listed units use polycarbonate materials that carry a 94V-0 UL rating.

### Safety is important

There has been a shift in manufacturing philosophy over the last decade regarding product power sourcing. Historically, power conditioning modules were built into the product, and a simple line cord supplied ac power to the product. Today, many OEMs design their products to operate on low voltage—typically 24V or less. External power supplies can readily supply these voltages directly.

Safety approvals from agencies such as UL, CSA, FCC, VDE, and IEC are vital to the success of any product that derives its power from a wall outlet. Depending on the sophistication and application of the product, the fees for agency approval can be substantial. Anytime the product is modified, the regulating agency must be notified. In many instances, the agency will require a resubmission of some kind. This means more engineering time and more fees for the agency.

It's obvious that approvals can be costly. Anytime a product is improved, the price tag for the modification could involve a good deal more than the cost directly related to the engineering change. Therefore, as the data in **Table 1** illustrates, external power supplies can create molehills out of mountains when it comes to safety.

Manufacturers of external power supplies essentially gain preapproval of OEM end products for the manufacturer by engineering standard approvals into their power-supply designs. External power supplies that are internationally approved reduce the need for full system approval in many areas. Manufacturers can shorten their development cycle by either reducing (or

## For more information . . .

For more information on the external power supply products discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in EDN.

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| -5.2V | ECL Logic | | | | ● | | | |
| -9V | Ethernet Communications | | | | ● | ● | | |
| -12V | RS232, Op Amps, RF Amplifiers | ● | ● | ● | ● | | ● | ● |
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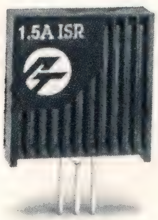

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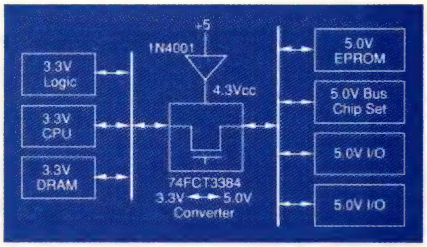

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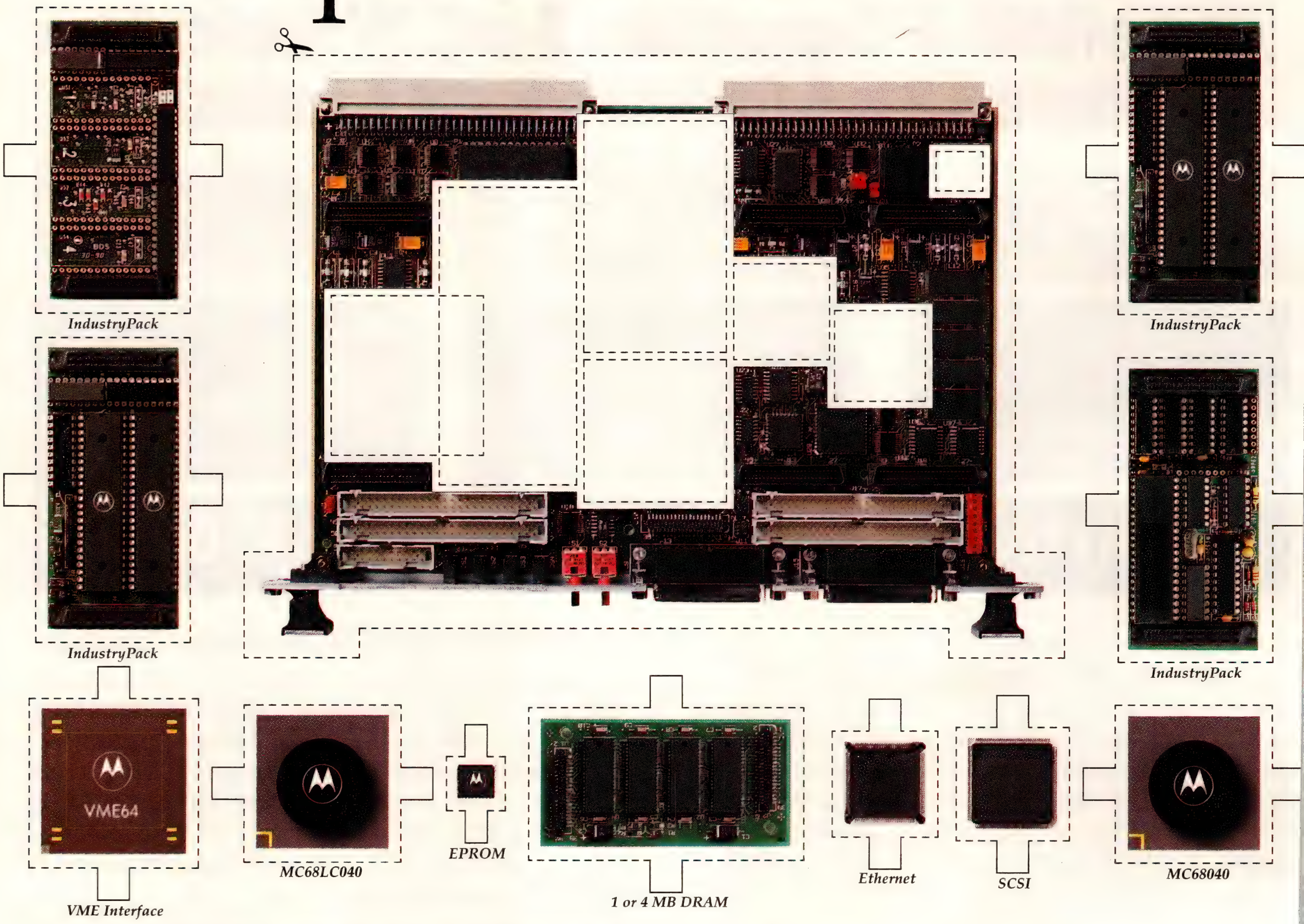

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CIRCLE NO. 42

# Boost programmable logic performance with timing-driven tools

**DOUG CONNER,** Technical Editor

**The best way to avoid timing problems at the end of a design is to use tools and methods from the start that help you meet your timing constraints.**

Of all the difficulties associated with choosing and using high-density programmable logic, whether field programmable gate arrays (FPGAs) or complex PLDs, meeting speed goals is often at the top of the list. Timing-driven design tools won't necessarily make speed problems go away, but they may help you extract better performance with less effort.

To understand timing-driven design tools and the benefits they offer, it's worthwhile to examine each step in the design process. By doing so we can try to sort out some of the general differences due to programmable logic architectures, and how the results differ between timing-driven and nontiming-driven tools. Each step in the process may be performed by automatic tools or the designer may perform them manually or interactively.

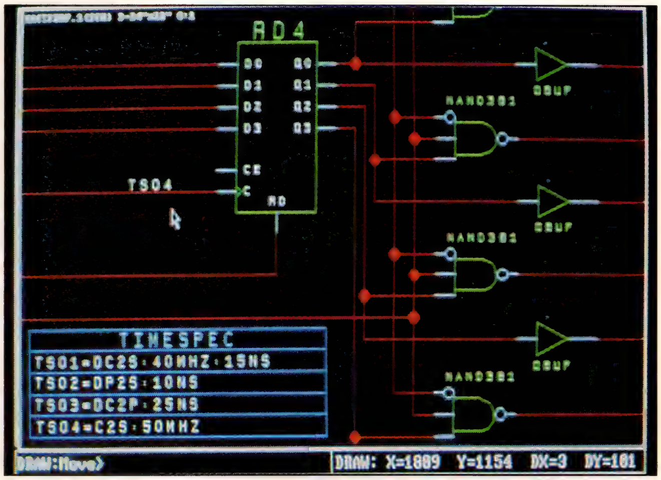
The programmable-logic design process from the point of view of timing can be broken down into four steps (see **Table 1**). The first step is to create the logic design using whatever methods are available and appropriate (VHDL, schematic entry, logic equations, etc) for your design. The second step is to map the logic into the logic-cell types of the programmable-logic architecture you have chosen. Next, you place the mapped logic into specific logic cells. The final step is to route the connections.

Each step in the design process affects the final timing, so you can't know what the timing is until the final routing step is complete. To add even more confusion, the timing effects at each step depend significantly on the programmable-logic architecture and the design tools you're using.

Even before you begin the logic design, you need a timing specification from which you can create solid timing constraints. An overall timing specification may boil down to a clock speed for getting data through one part of a system and into another. A specification may even be at a higher level, stating you need to perform some function on a set of data within a certain amount of time. In this case a clock speed would depend on whether you perform the function serially or in parallel.

### Logic architecture

The first stage of timing-driven design is using this high-level specification to come up with an architecture that



**XACT-Performance from Xilinx is a timing-driven place and route tool that lets you place your timing on the schematic as you create the design.**

will perform the function in a satisfactory amount of time.

Whether you're using a hardware description language and logic synthesis tools, equations, or designing at the schematic level, the basic architecture you or the synthesis tool develops will have a major impact on the timing of the system. Although the logic design has a significant effect on the design's final timing, the mapping, placing, and routing steps will add effects too.

Without timing estimates you'll need to perform many iterations through the entire design process to meet the timing constraints. All timing-driven design tools must have a way to estimate the effects a design decision will have on the timing of the design. The tools try to perform each step in the design process using timing estimates to control the design process to meet the timing constraints. Nontiming-driven design tools either have no mechanism for adjusting the design process to meet timing constraints or only do so indirectly.

Consider a design requiring a 32-bit adder. One of the simplest and most space-efficient implementations may be a 32-bit ripple-carry adder. A 32-bit ripple-carry adder is also relatively slow, requiring at least 32 logic-level delays, perhaps more on a fine-grained architecture. On some programmable logic architectures you won't know how many logic levels the device requires until you or the software tools have mapped the design. Although the ripple-carry adder is relatively slow, it may be fast enough for your design. You can add carry look-ahead logic to the adder and speed it up, but to do so unnecessarily will waste resources. You won't know unless you can estimate or compute the timing performance.

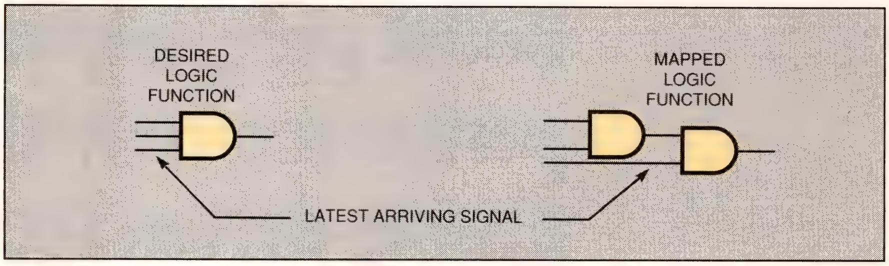


**Fig 1—The logic mapping shown places the late arriving signal in the most forward location, minimizing the effect of an added logic level on timing. The case shown represents a fine-grained FPGA architecture, but the same considerations apply to designs using multiple logic levels in complex PLDs.**

## Table 1—Timing effects in programmable-logic design

| Operation | Timing effect | |
|---|---|---|
| Logic Architecture:<br>Create logic design using design tools—schematic entry, hardware description language and logic synthesis, or equations and logic synthesis. | Gross architectural timing effects such as pipelined vs nonpipelined design, serial vs parallel operations, and state-machine encoding method. | |
| Logic mapping or fitting:<br>Translate logic architecture to logic-cell types available on selected programmable-logic device. | Determines number of logic levels in signal paths. Sets logic propagation delays. Routing delays are still unknown. | |
| | Field-programmable gate arrays | Complex PLDs |
| Place logic:<br>Assign logic to specific logic-cell locations. | Affects routing delays, but they are still not fixed. | Typically sets routing delays. |
| Route:<br>Connect logic and I/O cells as necessary to implement design. | Sets routing delays. | Typically a deterministic process with little or no effect on timing. |

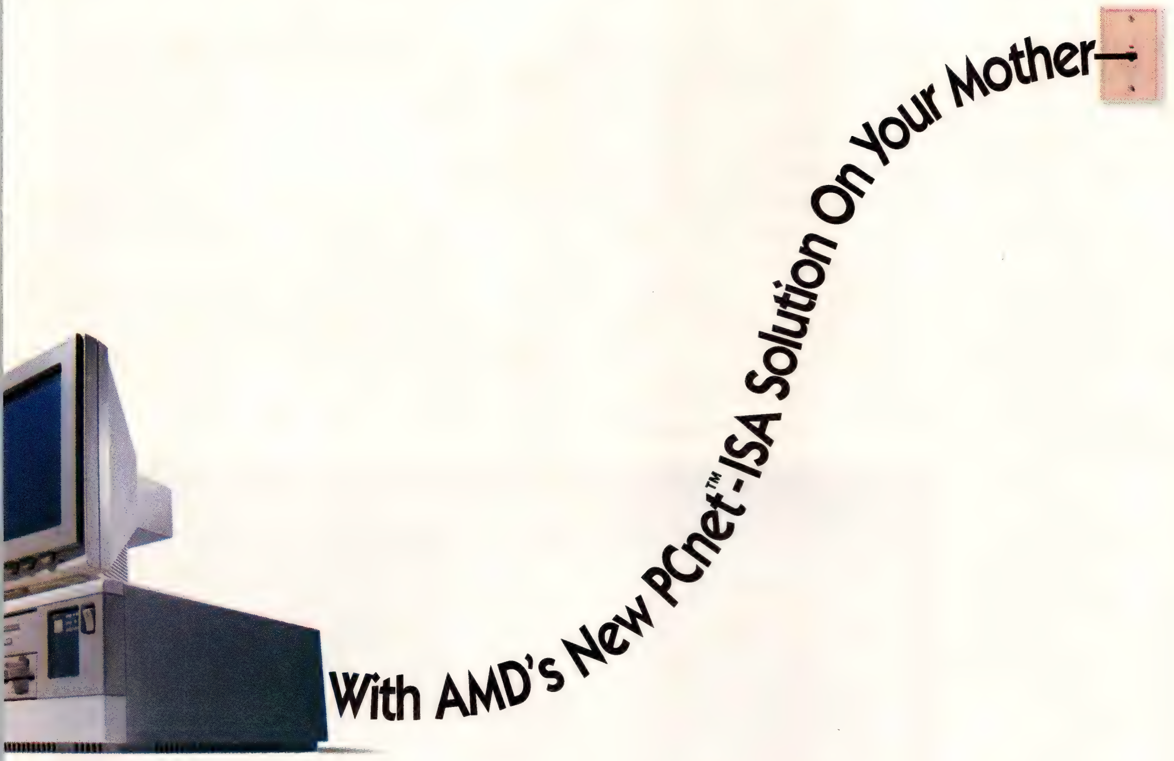
### Logic mapping

Even an estimate of the timing requires knowledge of how many logic levels are in a path. Fortunately, fitting or mapping logic into a programmable logic architecture is typically a fast operation. You may have the information available as you design, especially if you are designing at the schematic level. Many FPGA design tools provide macros that have predefined logic mapping. Complex PLDs with sum-of-products architectures can usually fit a large amount of combinatorial logic in a single level, simplifying timing estimation.

Although mapping is relatively straightforward, it can have an important effect on critical timing, especially when the path contains more than one logic level. **Fig 1** shows a simple example of how mapping affects timing. If you can bring in late arriving signals as far down a path as possible, you can avoid additional logic-level delays.

Note there are several reasons one signal may be later arriving than another. If one signal is later because it had to traverse more levels of logic than another, relatively simple mapping software should detect it and make the correct design decision. If a signal is later than another because it is the last bit to change in a counter down-counting to zero, you probably can't expect simple mapping software to detect it and map the design appropriately. Intelligent synthesis tools or the designer probably have to take care of this situation.

Once you have mapping information, you know how many logic levels a design uses. Returning to the example of a 32-bit adder used earlier, after mapping you know how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many logic levels are necessary to perform the 32-bit ripple-carry add. Using additional information such as logic propagation delays and typical interconnect delays for the device you're using, you can compute the typical time required for the adder to perform an add.

Data sheets for FPGAs can give you some typical logic-propagation and interconnect-delay information. Usually the logic-propagation delay based on fanout is relatively accurate. Typical interconnect delays vary considerably depending on the architecture. The classification of FPGAs covers a variety of architectures, some of which have more consistent and predictable interconnect delays than others. Examining the data sheets carefully will yield information on interconnect timing variations.

Another way to gain useful insight into routing delays is to examine in detail an automatically placed and routed design that uses up a substantial portion of the FPGA. Then you can see interconnect timing variations on a real design.

After mapping, but before place and route, fixed-routing-delay architectures offer much tighter estimates on timing. FPGAs and complex PLDs all offer more than one method of routing and have different delays associated with the different routing methods.

Even though placement affects the timing on complex PLD architectures, they have the most predictable and easiest to estimate timing in the design process.

If all this talk about estimating timing delays leaves you feeling that timing information is too indeterminate, you have an option on some programmable logic architectures. You can create hard macros for timing-sensitive parts of a design by placing and routing the macro logic on the device. The hard macro fixes the logic cell's interconnects and provides fixed timing. Devices with a regular structure of logic cells and interconnects let you move the hard macro anywhere on the device and maintain fixed timing.

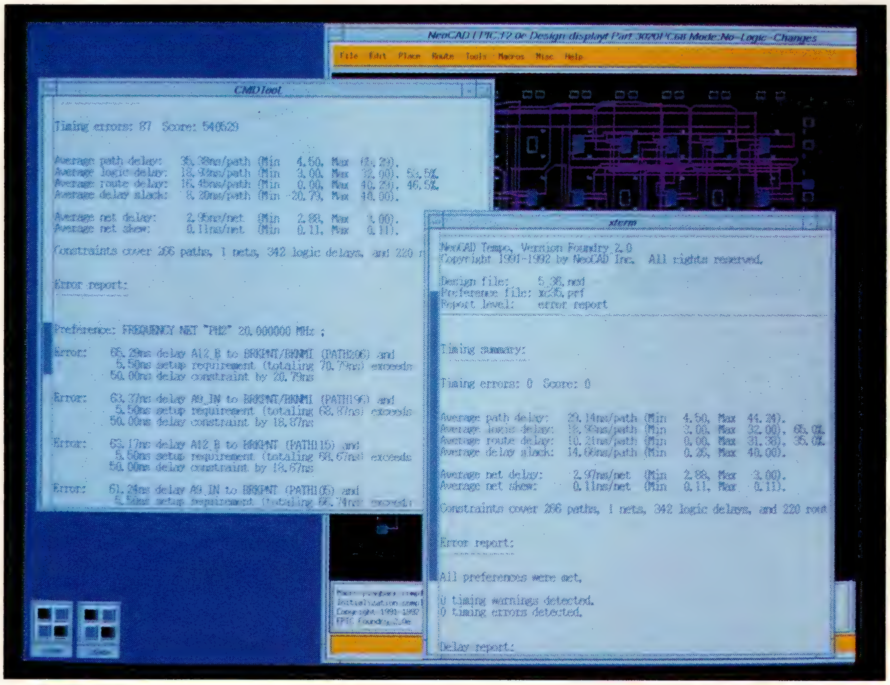
Continuing with the example of a 32-bit adder, once you map the design, estimate the timing, and add carry look-ahead stages if necessary to meet the timing constraint, you're ready to proceed to the place and route steps. Timing-driven design tools usually try to use resources to meet, but not to significantly exceed, the timing specifications. Good design requires a give and take of resources so a complete design will meet its specifications.

Before looking at the details of timing-driven place-and-route tools, let's examine how nontiming-driven place-and-route tools perform the operation. At the placement stage, automatic tools try to place logic in cells that are near other cells they connect with.

For FPGAs, the process is similar to placing components for a pc-board design. You can usually get most of the components to place with reasonably short connections, but some will have long connections. If you are using interactive placement tools for an FPGA design, you try to do much the same thing that automatic placement tools do, except you can put emphasis on keeping speed-critical logic close together.

With complex PLDs, the placement stage is relatively easy because placement within certain zones will have fixed timing. Some complex PLD architectures, such as Lattice Semiconductor Corp's (Hillsboro, OR) pLSI devices, have very small placement-dependent timing effects. Others have placement dependencies that resemble multiple, small, sum-of-product PLDs. Connections within one of the small PLD blocks will have one short interconnect delay. Connections that span between blocks will have a longer interconnect delay.

The next step is routing the design. On complex PLDs, once placement is complete, routing is a fast and automatic process whose effects on timing are already determined.


NeoCAD FPIC.F2 Design display Part 3020PC68 Mode:No-Logic-Changes
File Edit Place Route Tools Macros Misc Help
CMDtool
xterm

```
Timing errors: 87  Score: 540629

Average path delay:   35.38ns/path (Min  4.50, Max  65.29).
Average logic delay:  18.93ns/path (Min  3.00, Max  32.00). 53.5%
Average route delay:  16.45ns/path (Min  0.00, Max  40.29). 46.5%
Average delay slack:   8.20ns/path (Min -20.79, Max  40.00).

Average net delay:     2.95ns/net  (Min  2.88, Max  3.00).
Average net skew:      0.11ns/net  (Min  0.11, Max  0.11).

Constraints cover 206 paths, 1 nets, 342 logic delays, and 220 r

Error report:

Preference: FREQUENCY NET "PH2" 20.000000 MHz ;

Error:    65.29ns delay A12_B to BRKPNT/BRKMI (PATH206) and
           5.50ns setup requirement (totaling 70.79ns) exceeds
          50.00ns delay constraint by 20.79ns

Error:    63.37ns delay A9_IN to BRKPNT/BRKMI (PATH196) and
           5.50ns setup requirement (totaling 68.87ns) exceeds
          50.00ns delay constraint by 18.87ns

Error:    63.17ns delay A12_B to BRKPNT (PATH115) and
           5.50ns setup requirement (totaling 68.67ns) exceeds
          50.00ns delay constraint by 18.67ns

Error:    61.24ns delay A9_IN to BRKPNT (PATH105) and
           5.50ns setup requirement (totaling 66.74ns) exceeds
```

```
NeoCAD Tempo, Version Foundry 2.0
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Design file:     5_36.ncd
Preference file: xc36.prf
Report level:    error report

Timing summary:

Timing errors: 0  Score: 0

Average path delay:   29.14ns/path (Min  4.50, Max  44.29).
Average logic delay:  18.93ns/path (Min  3.00, Max  32.00). 65.0%
Average route delay:  10.21ns/path (Min  0.00, Max  31.30). 35.0%
Average delay slack:  14.60ns/path (Min  0.26, Max  40.00).

Average net delay:     2.97ns/net  (Min  2.88, Max  3.00).
Average net skew:      0.11ns/net  (Min  0.11, Max  0.11).

Constraints cover 206 paths, 1 nets, 342 logic delays, and 220 rout

Error report:

All preferences were met.

0 timing warnings detected.
0 timing errors detected.

Delay report:
```

**Timing-driven place-and-route tools that integrate data from top-level design through place and route, such as this one from Quicklogic, let you see exactly how automatic tools implement the design.**

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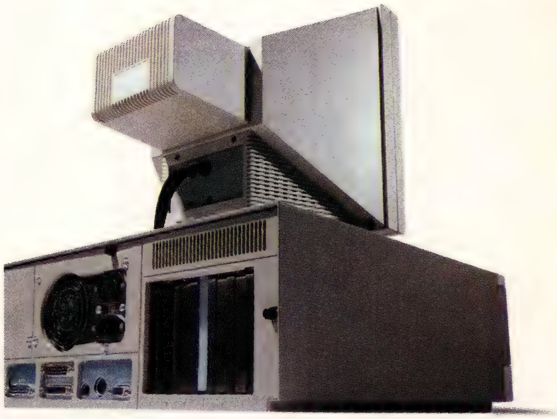

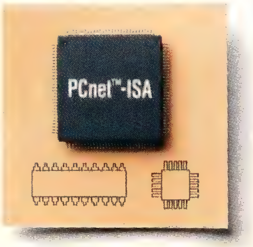

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FPGAs, or more specifically, programmable logic with channel-routed architectures, still have design work ahead that affects timing.

Nontiming driven tools attempt to connect all nets with as short a delay as possible while still fully routing the device. If the design automatically places and routes with timing that meets your needs, you are in good shape. If not, you usually have two general approaches. You can go back and prioritize nets to make critical nets have shorter delays. Or, you can use interactive tools to alter the placement or routing of the design.

Prioritizing nets is usually done one of two ways. One way is that you actually list nets in the order you want them routed (or at least those nets which you consider critical). The other way is to give nets some criticality rating that places them in groups of different priority.

Prioritizing nets works well in some cases for reducing interconnect delays, especially when the percentage of nets that need to be very fast is relatively low. You obviously have to be realistic in your expectations. You probably can't expect 50% of the nets to have the shortest possible delay. Also notice what the delay times are before trying to reduce them. If you are already getting the shortest interconnect delay the FPGA architecture can offer, no amount of prioritizing is going to fix the problem. You need to alter your logic design for greater speed or move the design to a faster device.

Achieving timing goals by prioritizing nets has two interrelated deficiencies that timing-driven place and route tools avoid. First, timing constraints are seldom net based. Usually they are path based. In a synchronous design (see **Fig 2**) you're concerned about the delay in a path between registers, not the delay in a particular net.

Timing-driven place-and-route tools let you specify delays based on paths and then try to create a placement and route that achieves the timing. The paths may be as short as a single net or as long as you need. Some timing-driven place-and-route tools such as those available from Xilinx and NeoCAD let you specify clock frequency and input and output paths, reducing

## Table 2—Representative timing-driven design tools for high-density programmable logic

| | | Timing-driven functions performed | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Manufacturer** | **Product** | **Logic architecture** (synthesis) | **Logic mapping** | **Logic placement** | **Routing** | **Programmable-logic family compatibility** | **Price** | **Notes** |
| **Crosspoint Solutions** | Crosspoint Design System | | N/A | ✓ | ✓ | Crosspoint CP20K | $12,950 | Fine-grained architecture does not require mapping because it has 1-to-1 mapping of gates' two logic cells. |
| **Exemplar Logic** | Core | ✓ | ✓ | | | Actel (Act 1, Act 2), Altera Max (5000, 7000), AT&T (AT&T 3000), Concurrent Logic (CLi6000), Crosspoint (CP20K), Cypress (Max 5000), Quicklogic (pASIC), Texas Instruments (TPC 10/20), Xilinx (2000, 3000, 4000) | $8000 (IBM PC)<br>$12,000 (workstation) | VHDL optional. |
| **Mentor Graphics** | Autologic | ✓ | ✓ | | | Actel (Act 1, Act 2), Altera Max (5000, 7000), AT&T (AT&T 3000), Cypress (Max 5000), Texas Instruments (TPC 10/20), Xilinx (2000, 3000, 4000) | $39,900 | Also Quicklogic link through NeoCAD VHDL optional. Product also supports ASIC design. |
| **NeoCAD** | FPGA Foundry with Timing Wizard option | | ✓ | ✓ | ✓ | Quicklogic (pASIC), Xilinx (3000, 4000) | $15,500 | Price is for FPGA Foundry, including Timing Wizard option. |
| **Quicklogic** | Spde 3.0 | | ✓ | ✓ | ✓ | Quicklogic (pASIC) | $2995 | Optimization is new in this release. |
| **Synopsys** | FPGA Compiler | ✓ | ✓ | | | Actel (Act 1, Act 2), Altera (Max 5000, 7000), AT&T (AT&T 3000), Crosspoint (CP20K), Texas Instruments (TPC 10/20), Xilinx (2000, 3000, 4000) | $25,000 (US Network license) | |
| **Xilinx** | XACT-Performance | | ✓ | ✓ | ✓ | Xilinx 4000 | $2000 | Frequent upgrade for existing XACT-4000 customers. |

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the need to specify every path in a synchronous design.

The second problem with using net priority to meet timing constraints is that you are using an indirect method to specify the timing you want. Using net-prioritizing methods, you may be able to create a place and route that meets the same timing constraints as you would with a timing-driven place-and-route tool. However, it's unlikely you'll be able to create the proper net priorities without several iterations. Timing-driven place-and-route tools let you specify system timing goals directly.

Going back to the 32-bit adder example, if you used a simple ripple-carry adder, you'd specify the timing constraint for the full path through the 32-bit adder. The time spent adding each bit isn't critical as long as the total path time was less than or equal to what you require. With a prioritizing scheme you have relatively indirect control. You could make every net in the path high priority, but that might be wasteful of fast interconnects.

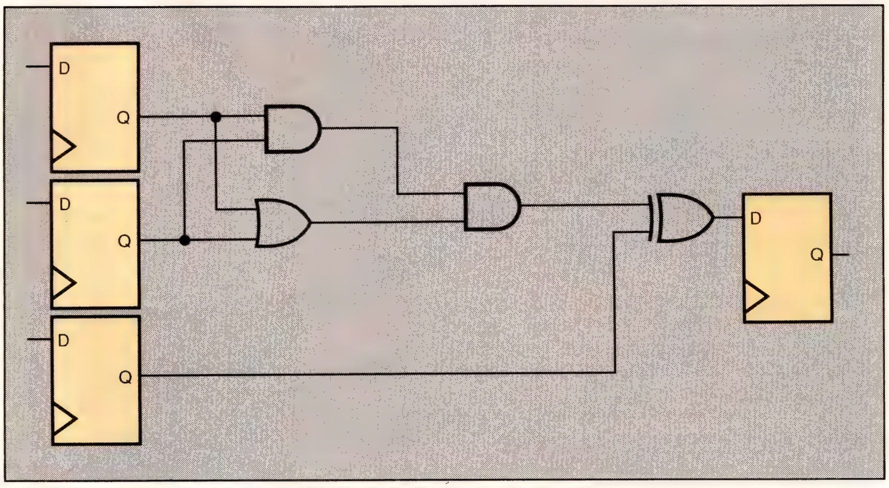


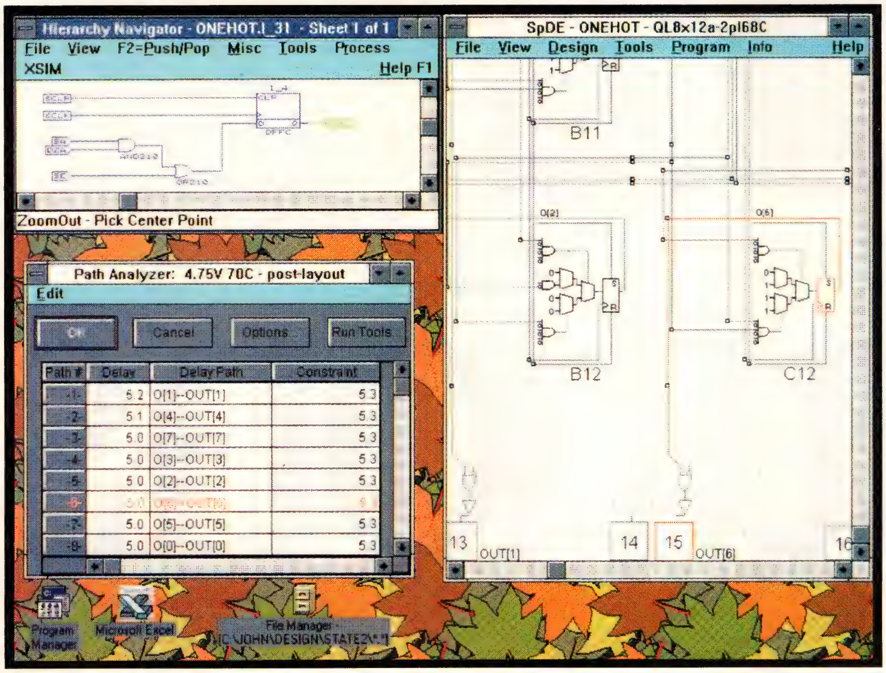
**Fig 2—Timing constraints are typically path-based, not net-based. In the simple example shown, the paths between registers are two to four nets long. Timing-driven tools let you specify path timing directly rather than trying to use net priorities. Individual net delays aren't important provided the design meets path delay constraints.**

Timing-driven place-and-route tools try to achieve a placement and route that meets timing constraints, but does not waste fast routing resources unnecessarily. If a path is much faster than necessary, the place-and-route tool may have used resources that another critical path needs. Perhaps the place-and-route tool could use slower routing resources or the logic cells associated with the path could be placed in different locations to offer shorter delays for other critical timing paths.

The specific algorithms used by timing-driven place-and-route tools are proprietary, but some general information will give you an idea of how they can achieve design improvements.

Slack time is a common concept in timing-driven design tools. It's used by both logic-synthesis and place-and-route tools. Once you've designed the logic and mapped it into the logic cells of the device architecture, you know how many levels of logic are in each path and the logic propagation delays. A timing analyzer estimates the typical interconnect delay.

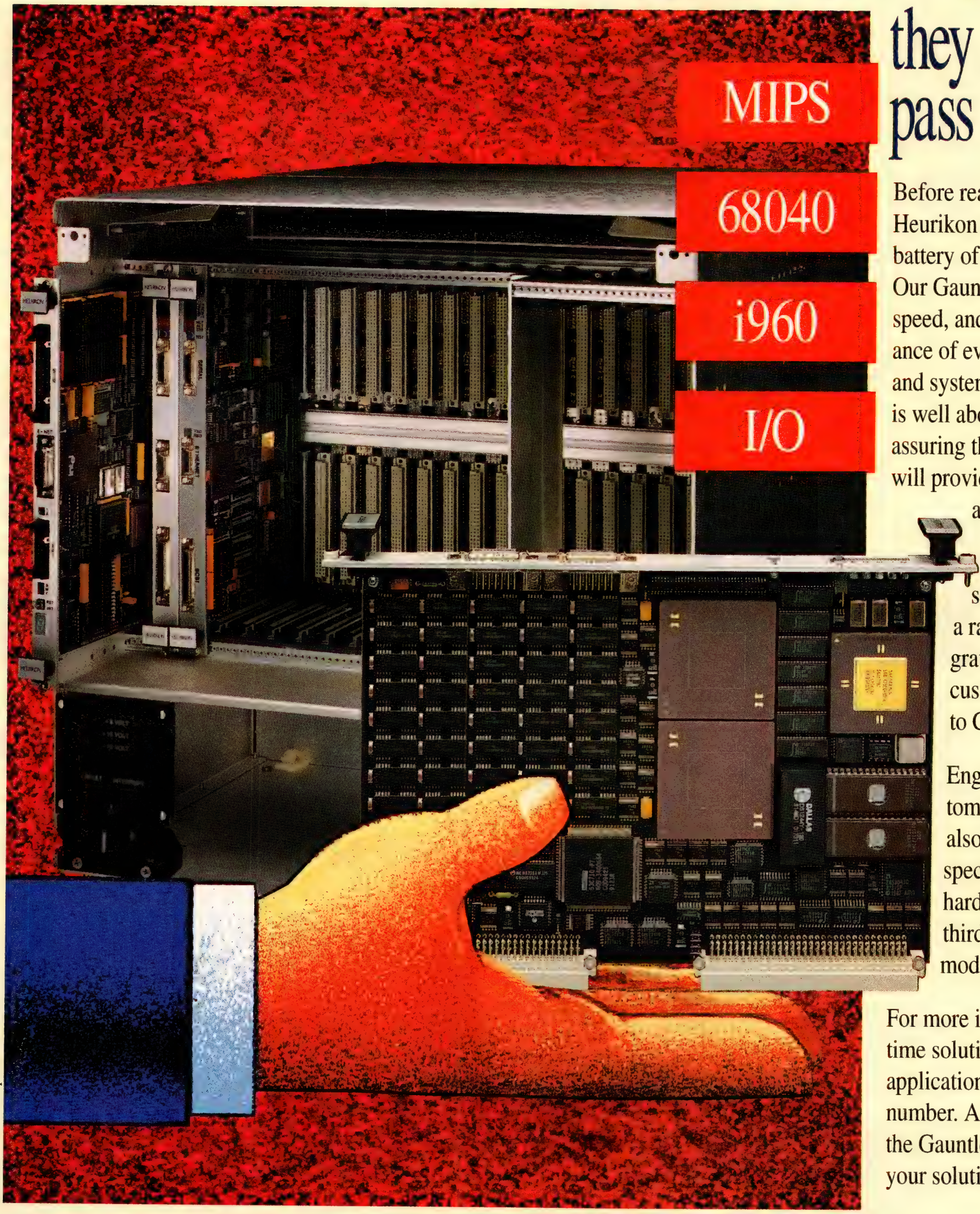
Using the estimated timing information, the software can compute the slack time for each path which is the maximum path-timing constraint minus the typical path delay. The software can also compute the average slack time per net by dividing the path slack time by the number of logic levels. If slack time is negative, the software can immediately flag the timing constraint as being tight. Slack time estimates based on the minimum interconnect



| Path # | Delay | Delay Path | Constraint |
|---|---|---|---|
| 1 | 5.2 | O[1]--OUT[1] | 5.3 |
| 2 | 5.1 | O[4]--OUT[4] | 5.3 |
| 3 | 5.0 | O[7]--OUT[7] | 5.3 |
| 4 | 5.0 | O[3]--OUT[3] | 5.3 |
| 5 | 5.0 | O[2]--OUT[2] | 5.3 |
| 6 | 5.0 | O[6]--OUT[6] | 5.3 |
| 7 | 5.0 | O[5]--OUT[5] | 5.3 |
| 8 | 5.0 | O[0]--OUT[0] | 5.3 |

**Timing-driven place-and-route tools that integrate data from top-level design through place and route, such as this one from Quicklogic, let you see exactly how automatic tools implement the design.**

# Before we call them Solutions they have to pass the test.



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CIRCLE NO. 45

delay can flag timing constraints as being impossible to meet with the current design. It won't waste time trying to place and route a design to meet an impossible constraint unless you direct the tool to just do the best it can.

Timing-driven design tools, whether at the architectural level or the place-and-route level, can use their timing-estimation capabilities to flag timing problems early so you can find and resolve timing problems earlier in a design. A logic-synthesis tool may change to a faster architecture to meet the timing constraint.

Armed with slack-time information for the paths, logic placement and routing priorities are reasonably clear and the automatic place-and-route tools can go to work.

## For more information . . .

For more information on the timing-driven design tools discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in EDN.

**Crosspoint Solutions**
5000 Old Ironsides Dr
Santa Clara, CA 95054
(408) 988-1584
FAX (408) 980-9594
**Circle No. 351**

**Exemplar Logic**
2550 Ninth St, Suite 102
Berkeley, CA 94710
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**NeoCAD**
2585 Central Ave
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(303) 442-9121
FAX (303) 442-9124
**Circle No. 354**

**Quicklogic**
2933 Bunker Hill Lane
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(408) 987-2000
FAX (408) 987-2012
**Circle No. 355**

**Synopsys**
700 E Middlefield Rd
Mountain View, CA 94043
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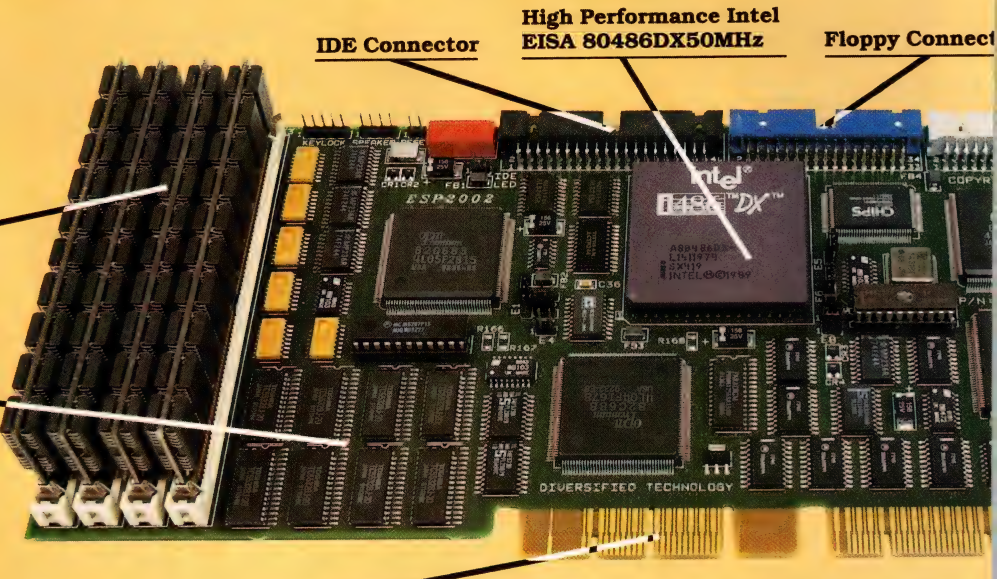
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For example, Crosspoint's timing-driven place-and-route tools for its FPGA architecture obtain optimum performance by packing logic with plenty of slack time close together. The routing software can resolve routing problems due to dense connection density by using slower interconnect paths without violating the timing constraints. The software places logic with minimal slack time loosely in the logic cells, providing abundant fast interconnect resources.

Of course timing-driven place-and-route tools may fail to meet your time constraints, but if they do, they flag the problems so you immediately can find the trouble.

Improvements in timing performance when using timing-driven design tools are sometimes impressive, especially if you aren't spending time interactively improving designs. Some of the companies contacted for this article claim numbers ranging from a conservative 10 to 30% improvement to numbers greater than 2x on specific designs. If you are already spending time interactively improving the placement and routing of designs, you may see the gain more in design time saved rather than absolute performance gains. EDN

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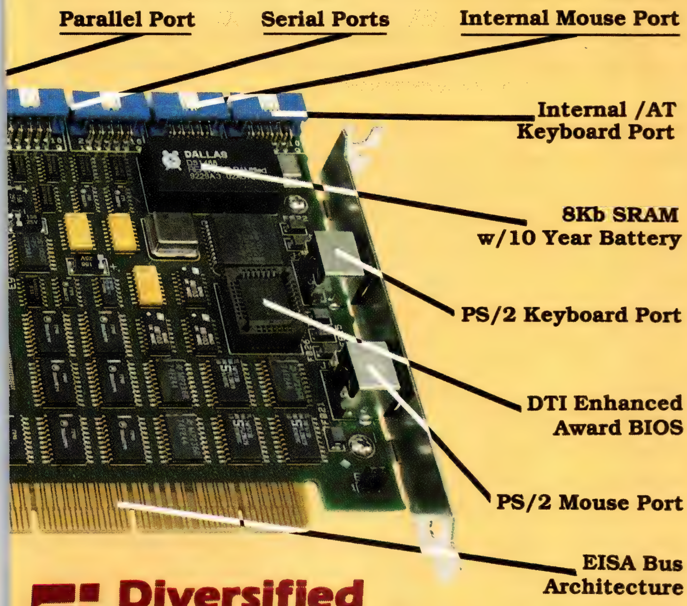

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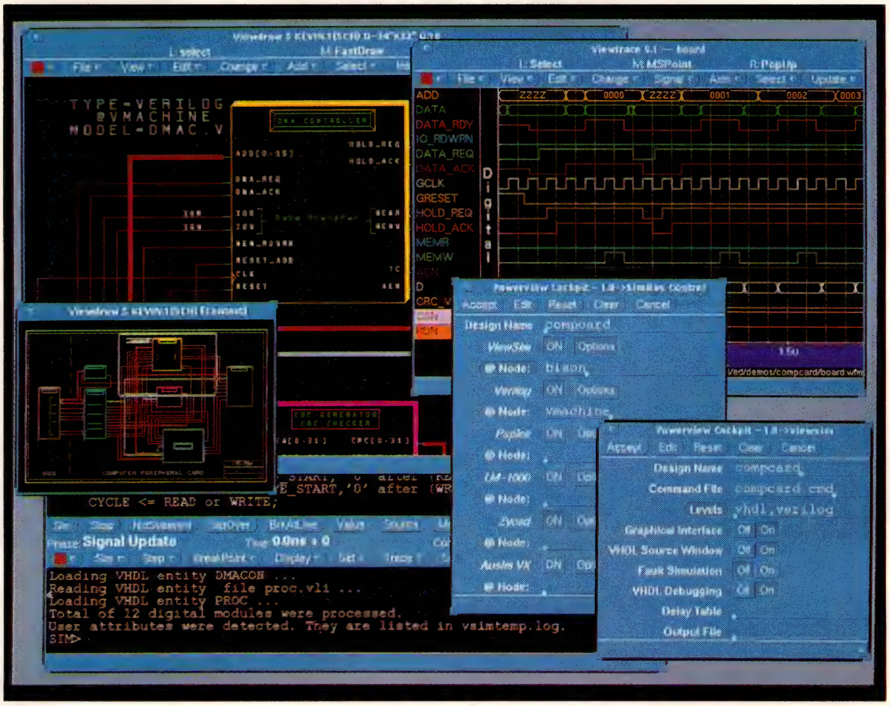
# Simulation backplane coordinates multiple simulators

You've designed a circuit, and you need to simulate different parts of it. But one simulator won't do everything you need to do or coordinate one kind of simulation with another. For example, you may want to simulate a critical path with a switch-level simulator, a section of random logic with a gate-level simulator, a state machine with a state simulator, and a register block with a behavioral simulator. Your options are limited.

You have two basic solutions. The most common is to simulate each piece separately. You can then build an appropriate model of each piece for subsequent simulations to run with other tools; or, you can mentally extrapolate the results for the subsequent simulations. However, because neither approach closes the loop between simulation and model, or simulation and extrapolation, they are both susceptible to errors. An alternate approach is to use hybrid simulators that may combine the capabilities of two simulators—most commonly switch-level (analog) and gate- or behavioral-level (digital) simulators.

Simulation backplanes or frameworks, introduced about three years ago by Mentor Graphics and Teradyne EDA (now Quickturn Systems), promised mixed-mode (analog/digital) and mixed-level (structural/behavioral) simulation capability by coordinating multiple simulators running concurrently. The technology had two limitations: The simulation-backplane vendor had to supply an interface for the particular simulators you wanted to use; and you had to partition your design among the appropriate simulators. In addition, the technology may not have made the best use of existing networked or multiple CPU hardware resources.

Simbus, a simulation backplane from Viewlogic Systems, addresses these partitioning and hardware-resource problems. Using automatic and semiautomatic modes, the software-based backplane identifies appropriate partitions using a master netlister, which interprets the design data and invokes subnetlisters for each simulator available on the backplane. Finally, to facilitate data transfer between individual simulators, the software inserts the appropriate interface logic between the various netlists.



```
E_START,'0' after (WR
    CYCLE <= READ or WRITE;
```

```
Loading VHDL entity DMACON ...
Reading VHDL entity  file proc.vli ...
Loading VHDL entity PROC ...
Total of 12 digital modules were processed.
User attributes were detected. They are listed in vsimtemp.log.
SIM>
```

Design Name compcard
Command File compcard.cmd
Levels vhdl,verilog

Fig 1—Simbus coordinates and reconciles multiple, concurrently operating simulators. Thus, you can choose the most appropriate simulator to evaluate each portion of your design.

The software uses available computer resources through two facilities. On a single-CPU system, semaphores signal the need for simulators to exchange data, rather than using a more wasteful polling scheme that requires simulators to ask each other whether they need to exchange information. The software can also start individual simulator processes on multiple CPUs. The software thus operates efficiently on multiprocessor computer systems. On a network, Simbus uses Unix sockets to monitor available computer resources and network loading. Viewlogic's testing has shown a 4 to 6% typical (10% worst-case) performance degradation over single-simulator runtimes on network-based operation.

The simulation backplane synchronizes all the various simulators via an event queue inside Simbus. The software converts all events to the Simbus queue and maps all converted events to each simulator's own event queue or system of equations. A benefit of these conversions is the greater accuracy and speed that results from every simulator's "knowing" what every other simulator is doing without having to back up.

The software allows you to choose your interface. If you are comfortable with the interface from a particular simulator, you can launch simulations from that tool, or you can use the individual interfaces for each of the simulators.

Although designers have always preferred to use the most powerful simulator for a project, their existing model libraries have often acted as an impediment to changing their current simulator. The high cost of redeveloping models for a new simulator has inhibited change. The ability to concurrently simulate old models on your current simulator and new models on the next-generation tool may lower that resistance.

Available now, interfaces to Simbus are written for Viewlogic's interpretive and Vantage Analysis Systems' compiled VHDL (VHSIC Hardware Description Language) simulators, as well as Verilog-HDL simulators from Viewlogic and Cadence, and Meta-Software's HSpice circuit simulator. Viewlogic will write interfaces, which can take 8 to 12 weeks to develop, depending on demand and backlog. The software license costs $6000.

The company has also announced CAE tools running under Windows 3.1. The suite offers design entry, simulation, and analysis modules. The software suits PLD, FPGA, ASIC, and system design using schematic capture and VHDL design-entry formats. System requirements are 12 Mbytes of memory and a 100-Mbyte hard disk on an 80386-based PC; pricing starts at $7500.—**Michael C Markowitz**

*Viewlogic Systems Inc, 111 Northbridge Rd, #11-04/06 Peninsula Rd, Singapore 0617. Phone (65) 336-6577. FAX (65) 339-5291.*

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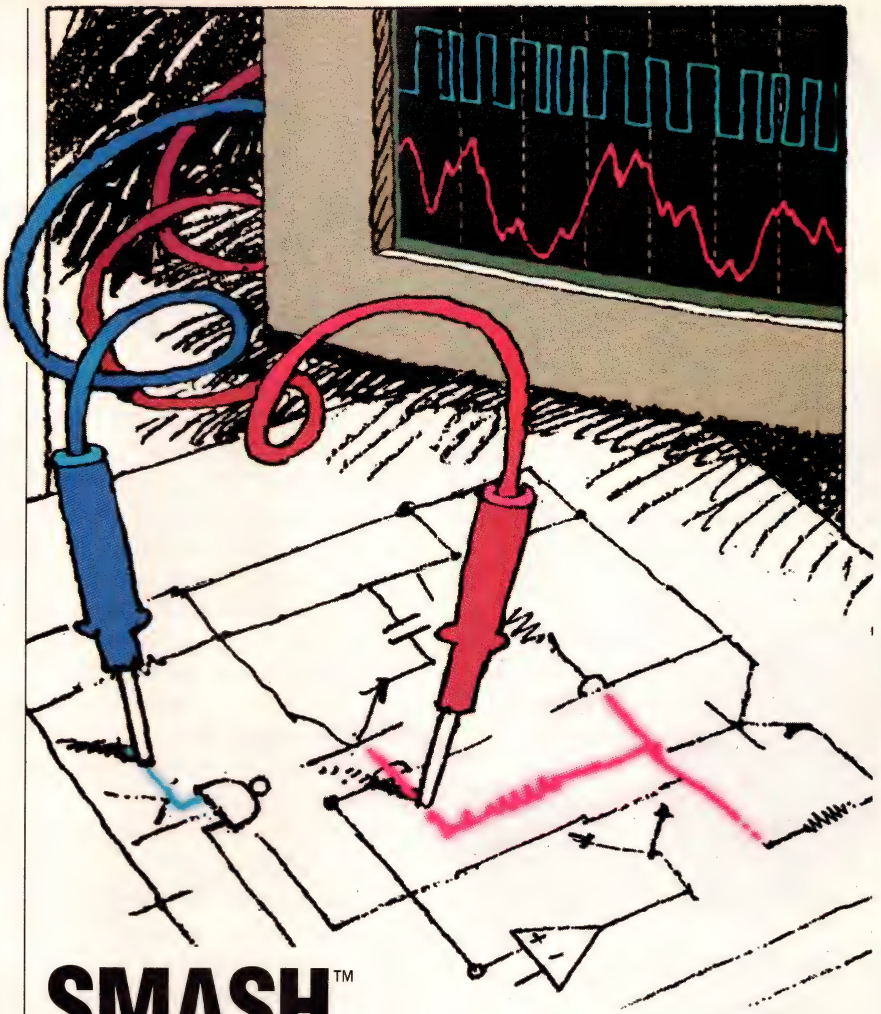
*Viewlogic Systems Inc, 293 Boston Post Rd W, Marlboro, MA, 01752. Phone (508) 480-0881. FAX (508) 480-0882.* **Circle No. 384**



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CIRCLE NO. 28

# FPGAs achieve PAL-device figures

Actel's latest family of field-programmable gate arrays (FPGAs) achieves performance figures comparable to a PAL device while providing the gate density and flexibility of an FPGA. Five devices of the Act 3 family, which are processed in 0.8-μm technology, provide gate densities ranging from 1500 to 10,000 gates and clock-to-output delays as short as 10 nsec. The devices enable on-chip 24-bit counter and state-machine designs exceeding 125-MHz clock rates.

The short clock-to-output delay allows signals to get on and off the chip quickly in high-speed designs. By utilizing the chip's short on-chip delays you can build a 75-MHz, 24-bit loadable counter; a 40-MHz, 24-bit accumulator; a 125-MHz shift register; and a 125-MHz, 24-bit prescaled counter. The family contains more than 350 macro functions, and it has 1153 dedicated flip-flops. The drive current for the I/O buffers is 12 mA, and the devices have four low-skew clock networks.

The family uses a propriety Plice antifuse programming-link technology. Unlike traditional fuse approaches, whereby programming creates an open circuit, programming an antifuse creates a low-resistance path. Because the antifuse is smaller than a metal-to-metal via, the devices can accommodate a large number of connections. For example, the A1460, a 6000-gate device, has 572,000 Plice antifuse elements. The ample wiring capability makes 100% automatic routing possible.

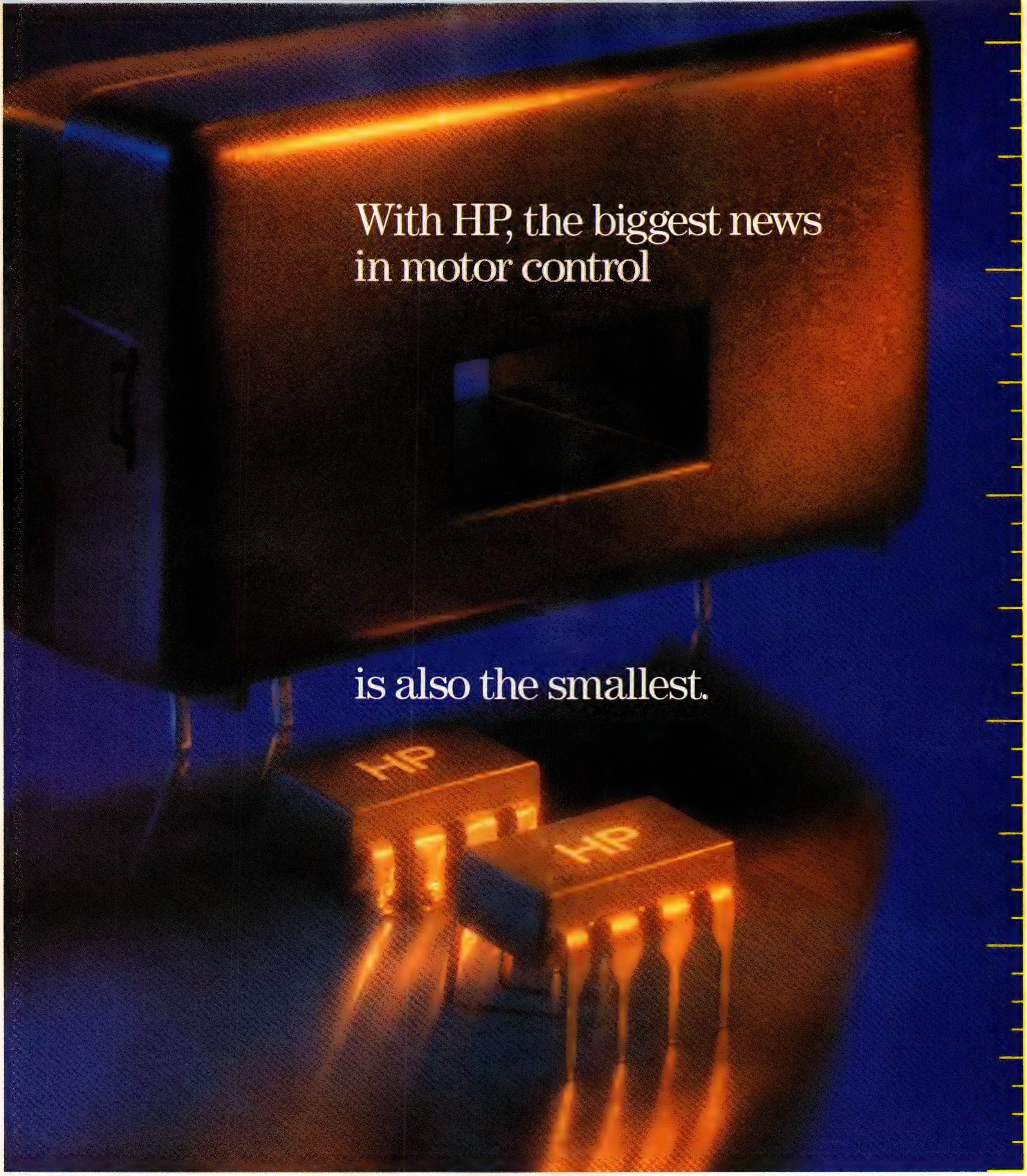
Actel has made architectural enhancements to its previous FPGA families to improve gate utilization. It has increased the horizontal tracks to 36 and the vertical tracks to 16. The enhancements make gate utilization as high as 80% and logic-module utilization as high as 95%. Also responding to customer requirements for higher I/O, the family provides a high pin-to-gate ratio. The five devices provide a range of 80 I/O pins and 1500 gates to 228 I/O pins and 10,000 gates.

**The Actel 0.8-μm Act 3 family of FPGAs achieves a clock-to-output delay of 10 nsec. The five devices have 1500- to 10,000-gate densities and can accommodate designs having 125-MHz internal clock rates.**

You can use the company's Action Logic System for quick turnaround FPGA designs. You can also use design tools from Cadence Design Systems, OrCAD, Viewlogic, Mentor Graphics, and Synopsis for your designs. The first available part-number and package prices (100) are A1425-PLCC (2500 gates), $79.30; A1425-PQFP (2500 gates), $99.60; A1460-PQFP (6000 gates), $272; and A1460-PGA (6000 gates), $342. The A1425 is available now; the A1460 is due in the second quarter of 1993.—**John Gallant**

*Actel Corp, 955 E Arques Ave, Sunnyvale, CA 94086. Phone (408) 739-1010. FAX (408) 739-1540.*

**Circle No. 382**



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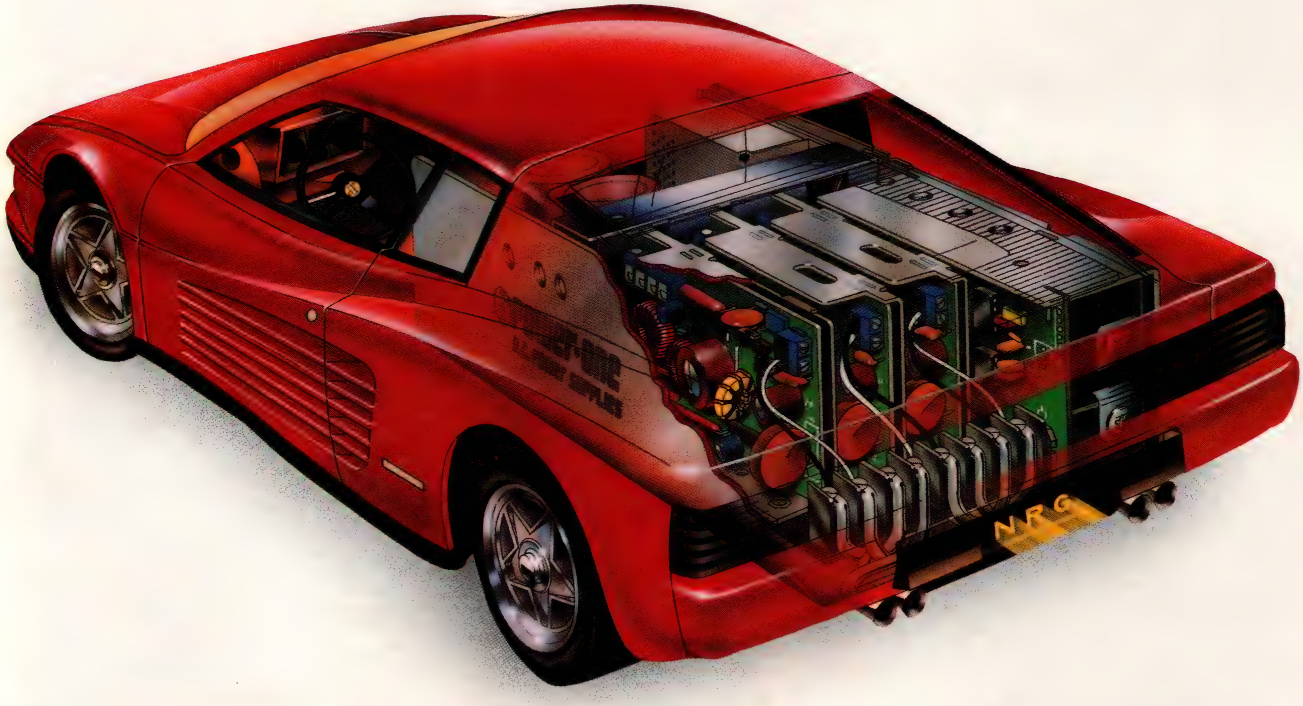

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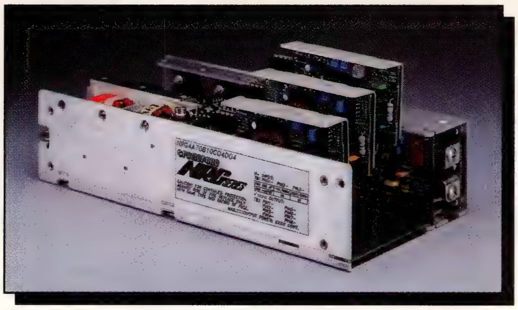

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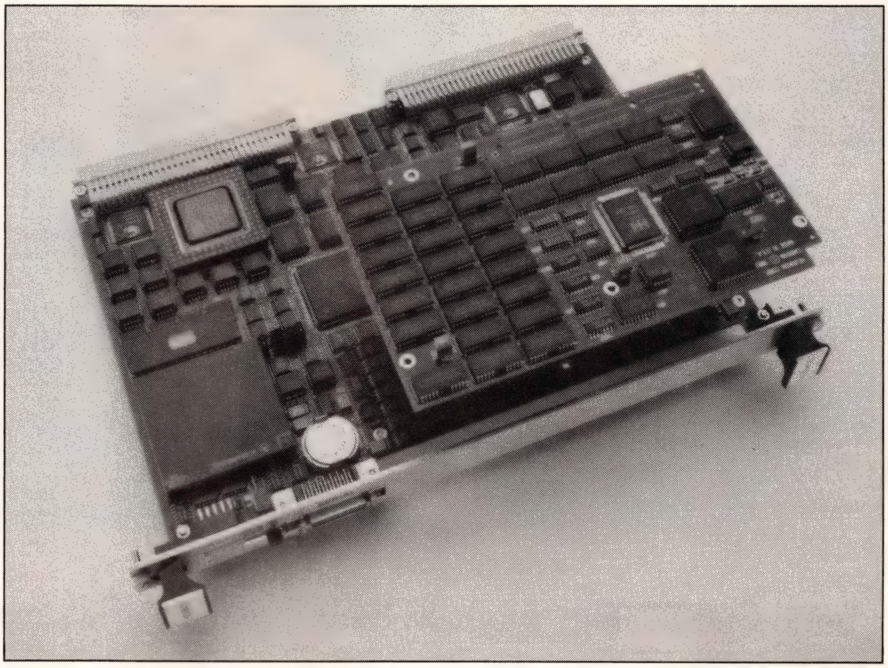
CIRCLE NO. 56

# 68040-based VME64 CPU board sports PCMCIA, Ethernet, and SCSI-2



**You can provide the HK68/V4D CPU board with custom memory and I/O capability via an optional 68-pin PCMCIA 2.0 plug-in module.**

If portability and customization in a VME64 format are important to you, you might consider the HK68/V4D CPU board. Built around a 33-MHz 68040 µP, this $4995 single-board computer provides a 64-bit, 60-Mbyte/sec Corebus mezzanine-card interface.

The Corebus interface is where you plug in the optional $600 HKCM/MIC PCMCIA (Personal Computer Memory Card International Association) 2.0 module. And into that module you can insert any of an array of memory, modem, fax, and I/O cards from a growing number of manufacturers. When mounted on a V4D baseboard, the module and board occupy a single VMEbus slot and provide a 200-nsec access time. An optional extender device with a 3.5-in. housing enables you to extend the PCMCIA socket to a front panel for mounting in a standard 3.5-in. peripheral bay. Paging software transfers parts of PCMCIA-based memory into the baseboard's RAM for faster execution.

The PCMCIA module is one of several modules available for the Corebus interface; other modules include the $2300 HKSEMEM8 8- or 16-Mbyte dynamic-RAM (DRAM) module. To assist designers who want to produce their own Corebus modules, the manufacturer also offers the $1000 Corebus designer's kit.

The HK68/V4D baseboard comes with 8 Mbytes of 2-way interleaved, dual-access DRAM with transparent hardware refresh and optional parity. You can upgrade this DRAM to 16 Mbytes. The board also comes with 1 Mbyte of EPROM, 4 Mbytes of flash EPROM, 512 bytes of nonvolatile RAM, three counter-timers, and a real-time clock.

The master/slave interface provides 32- and 64-bit block transfers as well as a 64-bit data path, 32-bit addressing, and slot-one system-controller functions. The interface also offers mailbox interrupts that enable remote control of the V4D for functions such as CPU reset, interrupt, and VMEbus lock.

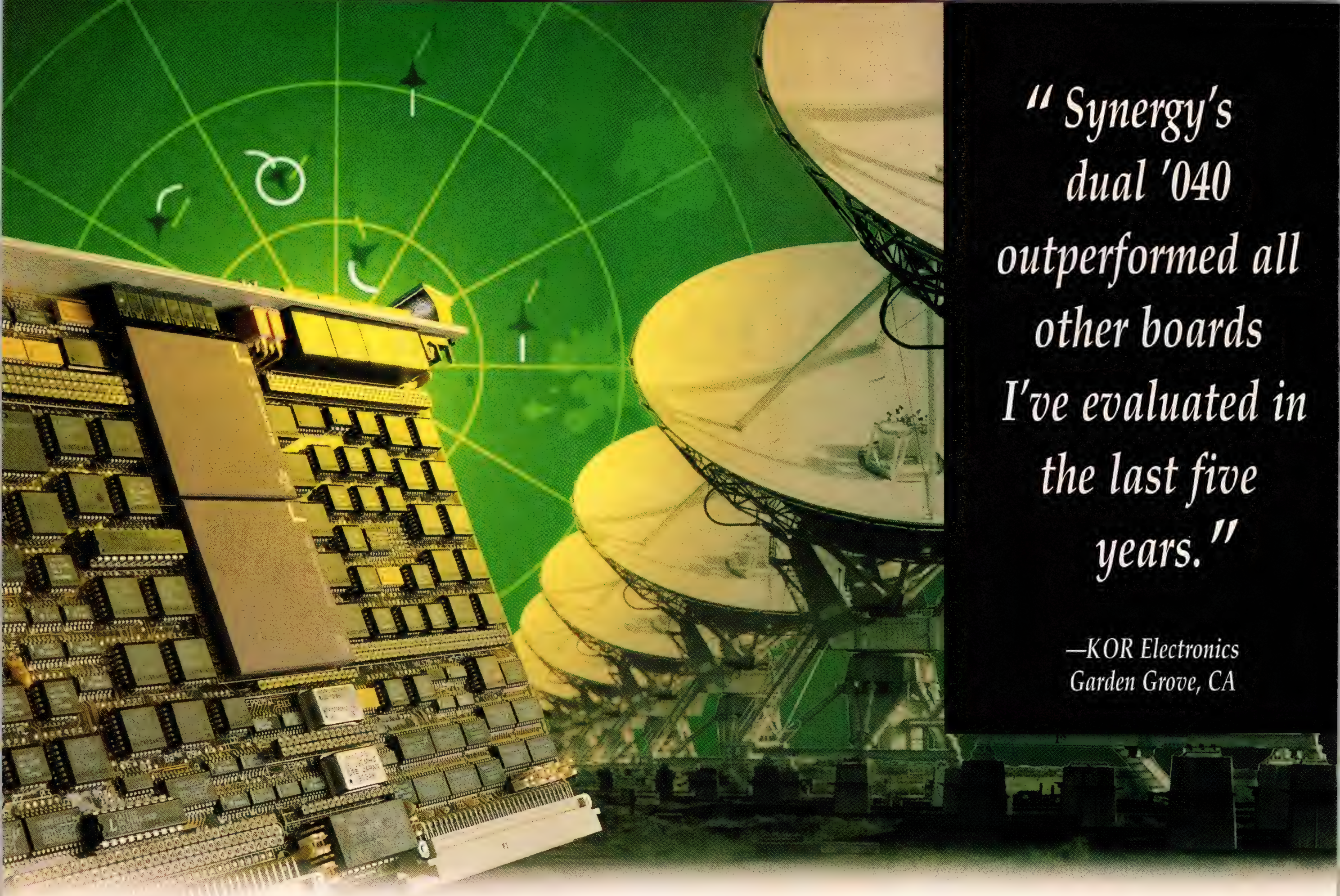
The onboard Ethernet interface yields 10-Mbps data-transfer rates, with FIFOs and an integrated DMA controller buffering and speeding data between the Ethernet LAN and the V4D's local Corebus. The SCSI interface works with as many as eight independent devices with 10-Mbyte/sec synchronous data transfers. A 32-bit DMA controller facilitates memory-to-I/O transfers without host-CPU intervention. The SCSI interface also permits data transfer in variable block sizes, 32-bit-word data bursts, and scatter/gather data transfers.

Additional I/O support for the baseboard includes a pair of serial I/O ports that offer RS-232C and RS-422 transfers with synchronous rates as great as 1 Mbps and asynchronous transfers of 38.4 kbaud. The two ports include an internal software-controllable baud-rate generator.

Software includes the manufacturer's Posix-compliant HK/Lynx real-time Unix operating system, VxWorks version 5.0, and Microware's OS-9 professional and industrial real-time operating systems.

**—J D Mosley**

*Heurikon Corp, 8310 Excelsior Dr, Madison, WI 53717. Phone (800) 356-9602; (608) 831-0900. FAX (608) 831-4249.* **Circle No. 385**



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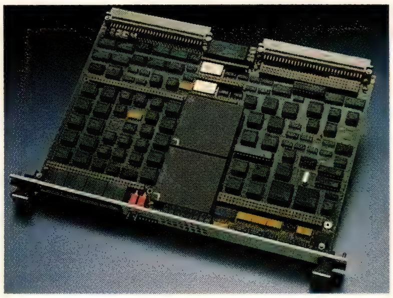

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CIRCLE NO. 67

# Roll your own TI DSP chip: Combine a C25 core and 15k-gate array

Many engineers find designing-in a DSP processor to be frustrating because DSP chips are generally not single-chip design options and require additional support chips. And, although DSP memory interfaces are relatively clean, DSP processors tend to lack single-chip peripherals. One solution is to use an application-specific DSP processor.

The Texas Instruments' cDSP (configurable DSP) chip combines TI's basic 16-bit fixed-point and 32-bit floating-point DSP (as cores) with tailorable ASICs. The TEC320C25A integrates an extended TMS320C25—a popular 16-bit fixed-point DSP—onto a 0.8-$\mu$m TI TGC1000 gate array. You get 15k usable gates for custom logic or to use as additional RAM or ROM.

The TEC320C25A builds on an extended TMS320C25 core. A second-generation 16-bit, fixed-point DSP chip, the C25 is an accumulator-based architecture with a single-cycle multiply-accumulate instruction. It competes with a number of 16-bit DSP processors, including Analog Devices' ADSP-2100, AT&T's DSP16, Motorola's DSP56156, and NEC's $\mu$PD77016. The C25 is now replacing first-generation TMS320C1x DSP chips. TI engineers extended the basic TMS320C25 by adding a software-controlled power-down mode to the C25, which enables the processor to drop power consumption while waiting for a power "WakeUp" signal to trigger an interrupt and resume processing.

TI engineers also added a PLL circuit for input clock control. This circuit enables designers to use lower-frequency board clock rates rather than the on-chip processor rates. The enhanced C25 core has a maximum frequency of 60 MHz, executing up to 15 native MIPS. The PLL circuit multiplies the input clock by 4; however, it can be bypassed by using a different clock input pin.

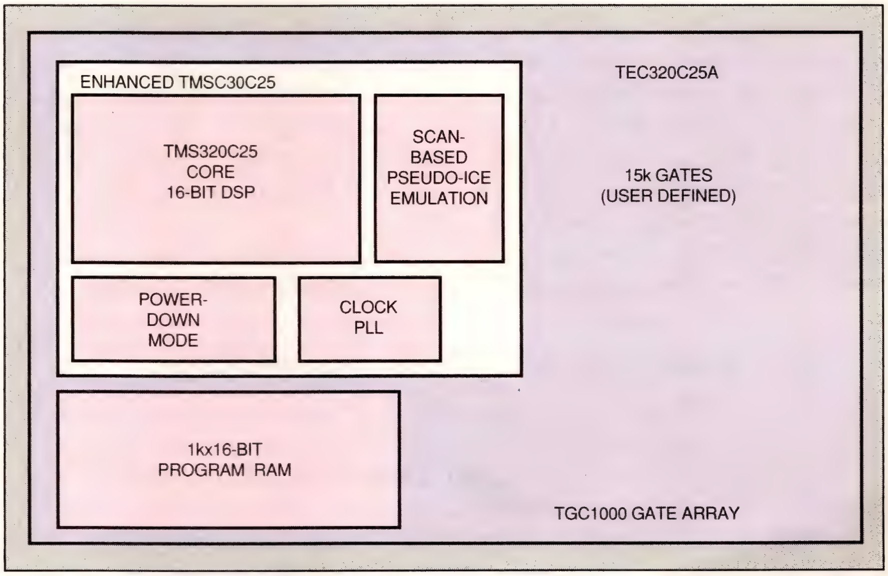
**TI TEC320C25A C25 core and gate array**

- 16-bit TMS320C25 DSP $\mu$P core with 4-kbyte ROM, 544-byte RAM
- 133 instructions
- 1k × 16-bit program RAM
- PLL clock to 60 MHz (4 clocks/instruction)
- Power-down mode to reduce power
- Scan-based, ICE-like emulation
- 15k usable gates (gate array)
- To 240-pin PQFP (100/144-pin QFP)
- From $75,000 NRE (prototype in 3 weeks)
- Parts, $15 to $25 (OEM qty)

The standard C25 core has 4 kbytes of ROM and 544 bytes of RAM, suitable for small application code or holding key inner-loop functions. The TEC320C25A adds 1k × 16-bit RAM to read-in and hold additional code, which can execute from on-chip memory. The C25 supports a 16-bit external memory interface with separate 16-bit data and address buses. To aid debugging, designers added a scan-based, pseudo-ICE capability from the TMS320C28, similar to that on TI's 32-bit DSP chips. Basically, serial lines enable users to take control of the processor: to single-step it, monitor and change register or memory values, and set software or hardware breakpoints.

The TEC320 Design Kit includes the TGC1000 Series gate-array library and a model of the C25 core. The model supports both Verilog and IKOS simulation models. A VHDL model is in development. Plans for the TI TEC320 cDSP family include adding A/D and D/A converters, as well as creating new chips that integrate the newer TMS320C5x and TMS320C31 DSP processor with gate-array logic. Both chips will run at 5 and 3V.

The cDSP family also includes DSP cores integrated with custom/standard cell technology. TI engineers combined the TMS320C31



**You can roll your own DSP chip with the TI TEC320C25A, which combines a C25 DSP $\mu$P with a 15k-gate array and 1k × 16-bit programmable RAM. Also added are a clock PLL, power-down mode, and serial pseudo-ICE control for debugging.**

DSP core with TI's 1.0-µm standard-cell TSC700 library. Prototype cycle time is typically six to eight weeks, slower than the 3-week turnaround for the TEC320C25 gate-array-based cDSP.—**Ray Weiss**

*Texas Instruments Inc, Semiconductor Group (SC-93002), Literature Center, Box 172228, Denver, CO 80217. Phone (800) 477-8924.*

**Circle No. 386**

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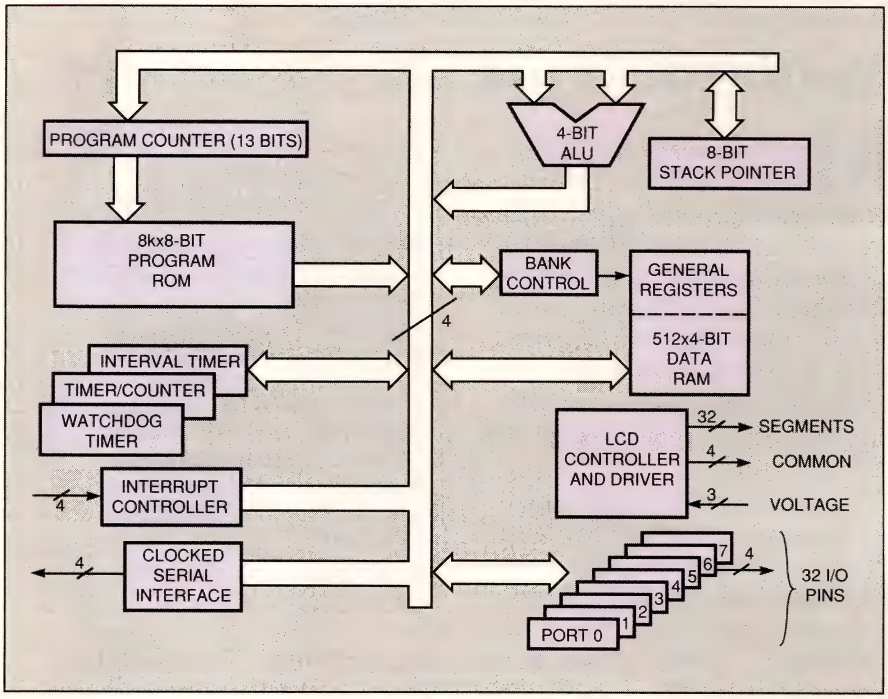
# 4-bit µC combines 2V operation and LCD drive



**This 4-bit µC drives up to 128 LCD segments without any external support chips. It has its own timers and accepts up to three vectored external interrupts.**

Four-bit microcontrollers (µCs) are not dead and buried. In fact, if you want a low-cost, low-power, single-chip design option with a range of peripherals, you might check out 4-bit µCs. These controllers particularly suit low-cost display applications, as there are not many 8-bit µCs that directly drive LCDs or vacuum fluorescent displays. If you need to drive 7-segment LCDs, take a look at NEC's µPD7530x, an upgrade of its 783xx family. It has an on-chip LCD controller capable of directly driving 32 LCD segments and operates to 2V for low power dissipation.

NEC's µPD75000 devices are not low-end CPUs; they provide a fairly high level of sophistication—in some aspects more than some low-end 8-bit µCs. The chips support vectored external interrupts, and they use memory-mapped peripherals, addressed as memory locations. Many chips have multiple timers with event and watchdog configurations. Like an 8-bit chip, program memory is byte-wide, with 1-, 2-, and 3-byte instructions. Unlike an 8-bit chip, the 75xxx series registers and ALU operations are 4 bits wide. But the CPU handles 8-bit arithmetic for wider addressing and allows code to address 8-bit accumulators (two adjacent 4-bit registers). Registers are held in local RAM, which is banked for easy addressing.

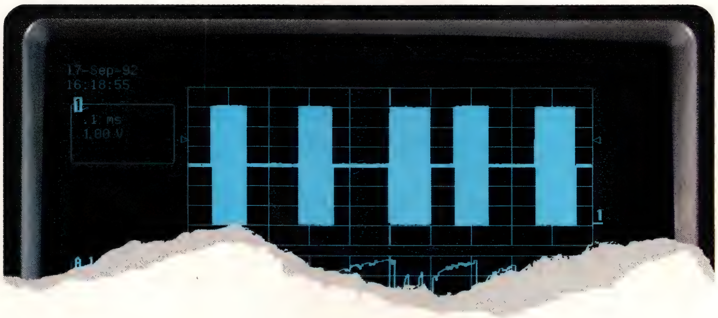
The µPD753xx µC has a built-in LCD controller with 32 direct (static-mode) segment drives. The controller can handle up to 128 segments by multiplexing the drive pins in conjunction with four phased backplane voltage levels. You can interface LCD segments directly with static or 1/2, 1/3, or 1/4 duty modes. In the multiplexed duty modes, each segment signal drives 2, 3, or 4 different segments in conjunction with phased backplane common signals. The chip interfaces directly with the LCDs and needs no support chips.

Running at 4.19 MHz and 2.5V, the chip takes a maximum supply current of 1.2 mA. Current can be cut further by reducing the chip's internal clock rate. The clock can be dynamically reduced by 4 or 8, with a corresponding reduction in power—CMOS chip power is proportional to the clock frequency. Or, operations can switch to the subclock, a 32-kHz base clock for background mode waiting (75 µA). For even lower power dissipation, you can go to stop mode, which stops the CPU clock and reduces supply current to 5 µA.

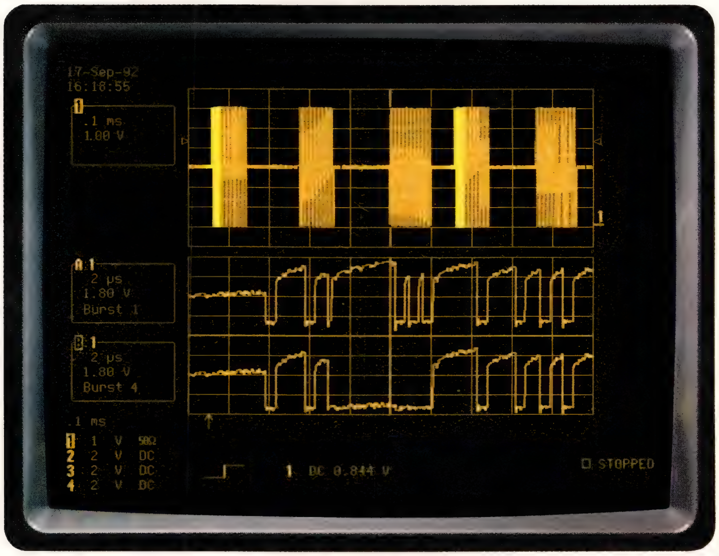
## Theory, operation, and application of LCDs

If LCDs are black magic to you, this free 100+-pg manual will give you the basics of 7-segment LCD technology and operation, as well as how to interface and drive them, including static (direct) drive and multiplexed drive (2-, 3-, and 4-duty operation). It describes LCD visual and ambient factors and how to interpret and use LCD manufacturer specifications. The text also details how to interface NEC's 4-bit µC to LCDs. All in all, this is a good addition to your design library. To receive a copy, phone the NEC Literature Center at (800) 632-3531.

# If you're only getting half the picture...



# ...talk to LeCroy.



Your analog oscilloscope gave you the whole picture. You'd set the trigger and the timebase, then use delayed sweep to examine the details. Measure precise timing. Or compare pulses in a stream.

But when you cross over to digital, will you still get the whole picture? Most digital scopes can't show you a live waveform and an expanded portion **simultaneously**. And if you can't see both together, how can you tell where the expansion really is?

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NEC's structured assembler simplifies assembly-language coding by allowing you to code in a high-level C syntax with statements such as IF/ELSEIF/ELSE, SWITCH, FOR, WHILE, UNTIL, as well as + +/− − increment and decrement and a C-like preprocessor. NEC supplies an ICE for the chip family.—**Ray Weiss**

*NEC Electronics Inc, 401 Ellis St, Mountain View, CA 94039. Phone (415) 960-6000.* **Circle No. 387**

**NEC µPF75308B 4-bit µC**

- 4.19-MHz clock (32-kHz subclock)
- 4-bit ALU; 4-/8-bit operation
- 0.95-µsec cycle (1-byte instruction)
- Accumulator-based CPU (4/8 bits)
- 8 4-bit (or 4 8-bit) RAM-based registers
- 4 to 8k×8-bit ROM/OTP/EPROM
- 512 4-bit "nibble" data RAM
- 3 8-bit timers; serial interface
- 2 to 6V operation
- LCD controller direct drive for 32 segments; works with 1/2, 1/3, 1/4 duty operation (max 128 segments)
- 40 I/O pins, 3 external interrupts
- 8-kbyte, 80-pin PQFP, $4.20 (10,000)

---

# µC integrates 8-/16-bit processing with LCD controller

Hitachi's H8/3834 integrates an 8-/16-bit CPU with a raft of peripherals, including five timers, a 14-bit PWM device, three serial ports, an 8-bit A/D converter, 13 external interrupt pins, and an LCD controller. The LCD controller has 40-segment drive pins. With a full peripheral set, the H8/3834 handles many handheld consumer applications.

The Hitachi H8/3xxx is basically a 16-bit µC with an 8-bit external bus and is priced at the high-end of 8-bit µCs. Competition for the H8/3834 includes NEC's K0 family, which integrates 4-bit peripherals with an 8-bit µC, and Motorola's 68HC05 family, with on-chip LCD drive parts. The H8 has the advantage of a large program ROM/EPROM—up to 32 kbytes for large single-chip applications and 1 kbyte of data RAM.

Built on an 8-/16-bit CPU, the H8/3000 processor features a 16-bit ALU with eight general-purpose 16-bit registers (also addressed as 16 8-bit registers). The µC addresses a unified 64-kbyte memory space; the chip has a 16-/8-bit external address/data bus for external memory. Program memory is 16 bits wide on chip, which is a speed advantage, as most instructions can be fetched in a single cycle.

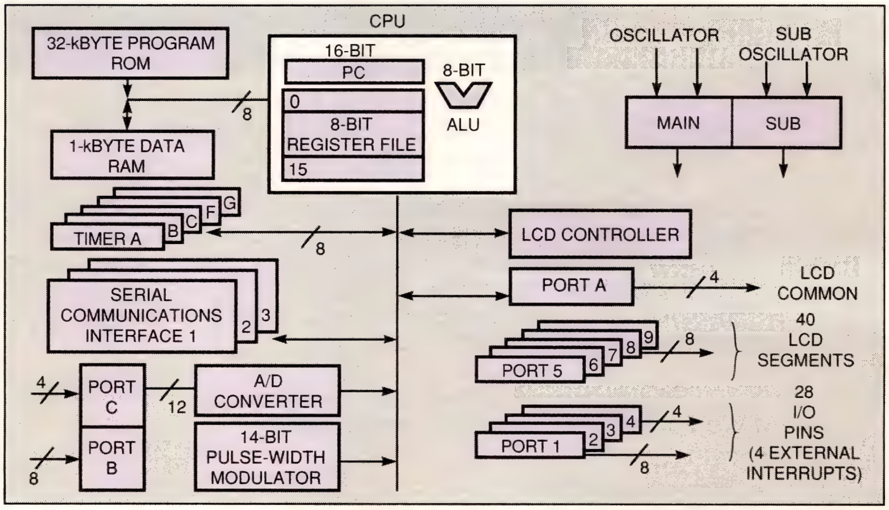
Programming the H8's CPU is relatively straightforward. The processor provides eight addressing modes, including register and memory indirection, which make programming much easier. Even better, register indirect works with predecrement or postincrement options for easy indexing and looping. The instruction set is orthogonal, based on operating on a general set of registers.

**Hitachi H8/3834 8-/16-bit µC**

- 10-MHz internal clock
- 16 8-bit or 8 16-bit registers
- 16-bit ALU, 16-/32-bit instruction word
- 200-nsec ADD; 1.4-µsec MPY, DIV
- 57 instructions
- 64-kbyte address space
- 1-kbyte RAM; 32-kbyte ROM
- 14-bit PWM timer
- 4 8-bit timers; 1 16-bit timer
- 8-bit A/D (12 input channels)
- Interrupts: 13 external; 21 internal
- LCD controller; 40 segment drivers (direct, 1/2, 1/3, 1/4 duty ratio)
- In 100-pin PQFP, ROM version, $9 (10,000); OTP version, $15 (5000)

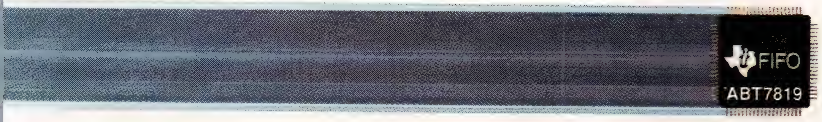
H8/3834's on-chip LCD controller can drive up to 160 7-segment LCD segments (1/4 duty). The controller handles direct (static) 1/2 (duplex), 1/3, and 1/4 duty segment multiplexing. The 40-segment drive signals can be shared by different segments in a multiplexing scheme that varies the four backplane signal phases. Phase differences between the frontplane segment lines and the backplane signals enable a single segment line to drive up to four LCD segments without any external chip support. With external extension logic, the 32-segment drive lines can drive up to 520 LCD segments.—**Ray Weiss**

*Hitachi America Ltd, Semiconductor & IC Div, 2000 Sierra Point Pkwy, Brisbane, CA 94005. Phone (415) 589-8300. FAX (415) 583-4207.* **Circle No. 388**



**The Hitachi H8/3834 8-/16-bit µC drives up to 160 LCD segments directly; it accepts 13 external interrupts and has 5 timers, an A/D converter, and a PWM device.**

# FASTEST IN.



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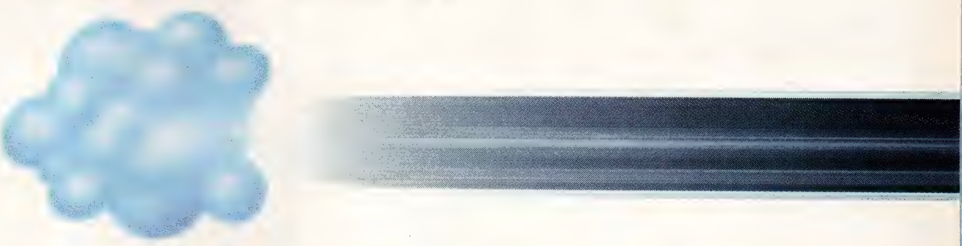

# THE NEW 80-MHz 'ABT7819 FIFO FROM TEXAS INSTRUMENTS.

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## Blazing speed with excellent metastable characteristics

Based on our power-saving Advanced BiCMOS technology, the 'ABT7819 has a maximum access time of 9 ns (measured at $C_L = 50$ pF). It's the first to offer such performance. And its unique multistage synchronization circuitry greatly improves the metastable characteristics of status flags. That makes it an excellent choice for today's high-speed multiprocessing systems—or any system where speed and reliability are paramount.

**BIDIRECTIONAL FIFOs**

| Device | F max (MHz) | Max access time (ns) | Data setup time (ns) | Data hold time (ns) |
|---|---|---|---|---|
| 'ABT7819 | 80 | 9* | 3 | 0 |
| '72615[†] | 40 | 15 | 6 | 1 |
| '5420[‡] | 40 | 16 | 12 | 0 |

* $C_L = 50$ pF vs. standard 30 pF test load.

Specs based on manufacturers' data as of April 1992,[†] July 1992[‡]

## Highly integrated in a choice of standard packages

The bidirectional 'ABT7819 is more than just two 512-word-deep by 18-bit-wide FIFOs sitting side by side. It's bidirectional control logic, flag logic, latches and synch circuitry integrated into a single package to simplify your designs.

The 'ABT7819 comes in compact 80-pin SQFP (actual size 14 mm x 14 mm tip to tip) and standard QFP packages to help save valuable board space. Plus, it's available in −12-, −15-, −20- and −30-ns cycle times for easy performance upgrades.

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For more information on the SN74ABT7819, use the reader service number below or contact your local TI sales office. We'll have you up to speed in no time.

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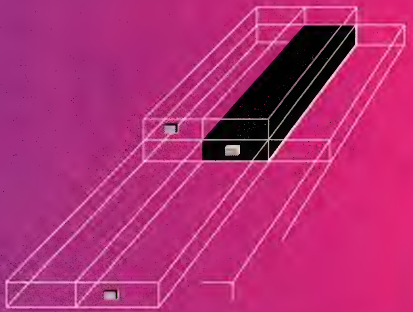
|---|---|---|---|---|---|---|---|---|
| | | | Charging Current (mA) | Time (Hrs.) | L (mm) | W (mm) | T (mm) | |
| | 1.2 | 600 | 60 | 14-16 | 67.0 | 17.0 | 6.1 | 23 |
| KF-B400 | 1.2 | 900 | 90 | 14-16 | 67.0 | 17.0 | 8.1 | 30 |
| | | | | 14-16 | 67.0 | 17.0 | 10.3 | 38 |
| | | | | 14-16 | 48.0 | 17.0 | 8.1 | 21 |
| | | | | | 48.0 | 17.0 | 6.1 | 16 |

CIRCLE NO. 60



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| PQFP | 16 SOIC | 28 PLCC | 44 PLCC | 68 PLCC | 84 PLCC |
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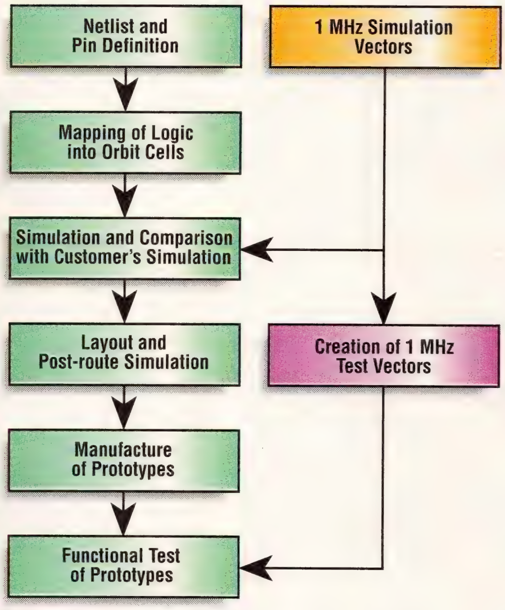

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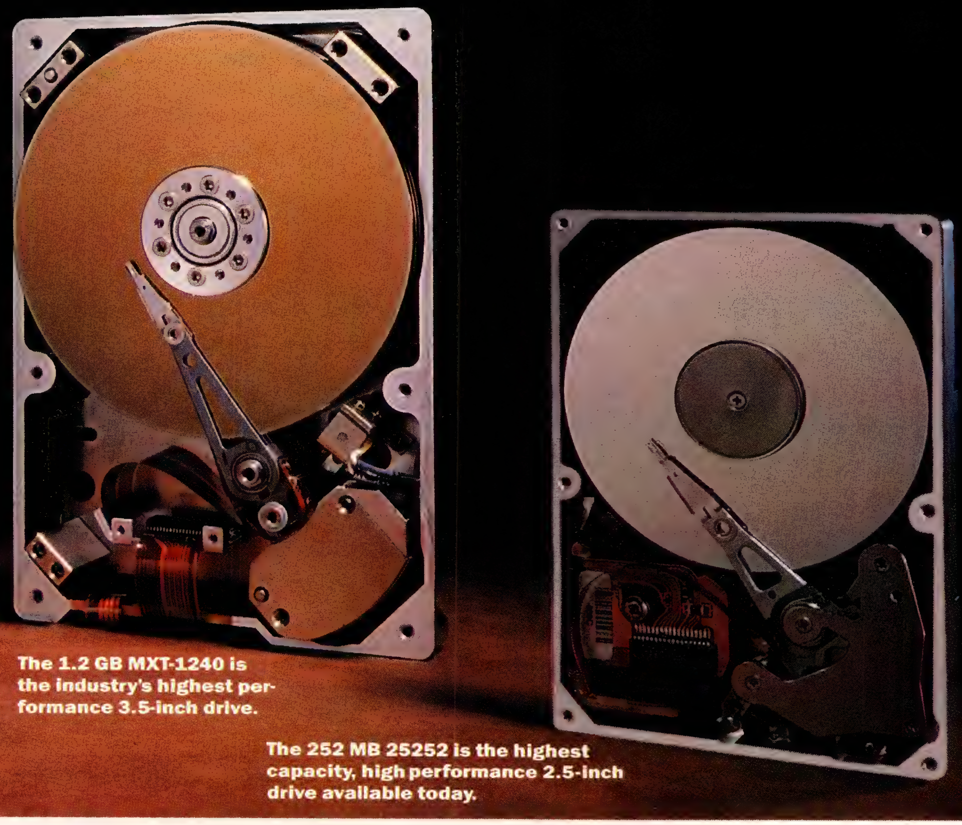

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CIRCLE NO. 62

# STAYING AFLOAT
## in high software seas

Million-line software projects differ from small ones, and not just in line count for code and head count for the development team. You need additional tools and a new set of rules to keep your head above water while programming-in-the-large.

**JOHN C NAPIER, Technical Editor**

"Quantity has a special quality all its own," said Joseph Stalin. Those of us who pursue technology more fervently than politics might say he was addressing the issues of combinatorial and structural complexity. In other words, new types of problems come up in practical dealings with large numbers of anything, including lines of code. Developing a million-line program isn't the same as writing a hundred 10,000-line programs. Four examples of million-line programs—a PC-based CAE tool, workstation-based CAE tool, software that

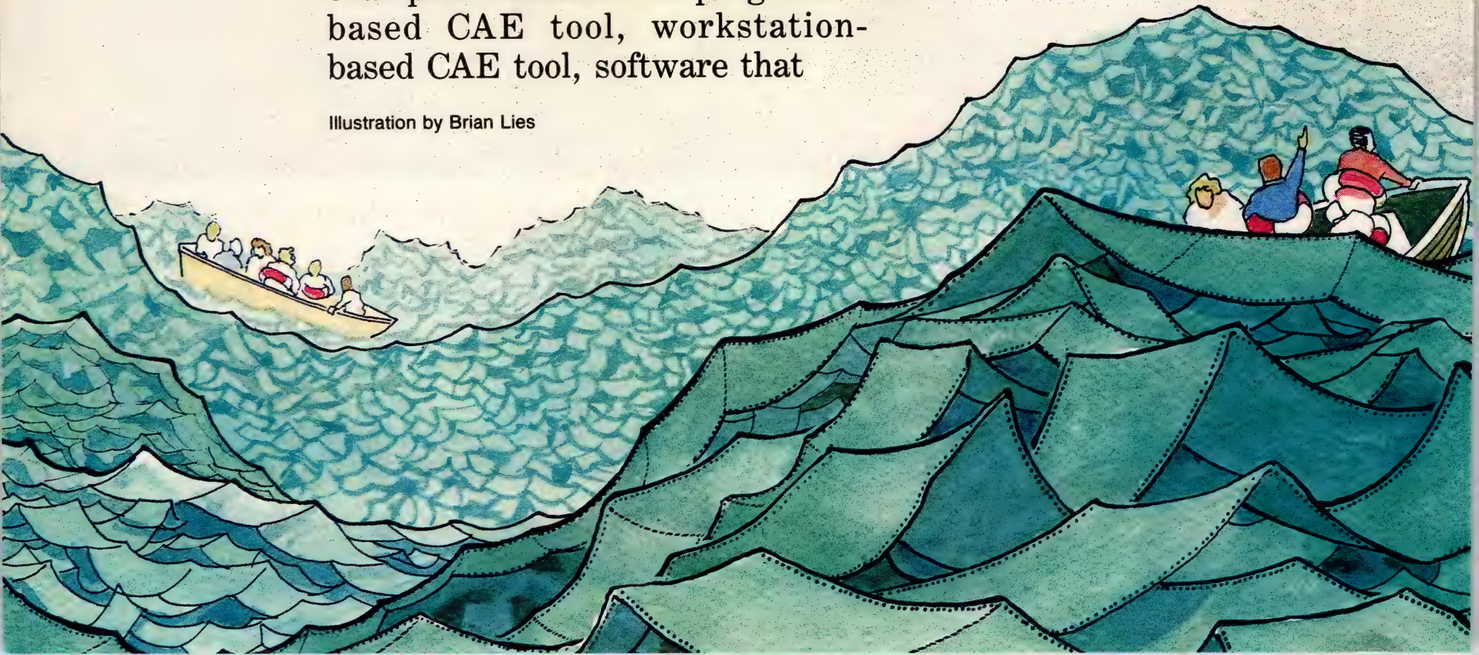


Illustration by Brian Lies

TEMPLATES
REPOSITORIES
CODE BROWSERS
BL

controls a small warship, and software that pilots a commercial airliner—will show how developers meet the challenge.

The differences between working on a small program and working on a very large one fall into two categories: team size and tool type. First consider team size: Small programs rely on the memory of one individual to organize their complexity. Assuming that each person added to a team communicates in some way with every other person, you'll find that the number of possible conversations increases approximately as $n^2/2$. This calculation puts some numbers to how team members change the way they communicate as team size grows. Five or six people communicate by informal memo-passing. Twenty to thirty people use—or should use—software tools to help control complexity. Examples of such tools are source-code control and configuration-management tools.

Projects of 200 to 2000 people working on a program need a distributed CASE environment with a repository for capturing information from all phases of development, not just code. As the size of a program and team increase, it becomes important to capture relationships between documents in addition to organizing them by name and category. Continuity over time is also an issue for large teams. Tasks such as scheduling backup and updating a repository database have to be planned carefully.

Second, tool types. People use more specialized tools on large programs. They use them not just to save labor or because the overhead budget will support the purchase, but because large programs impose an exponentially increasing penalty for defects.

To determine whether you're dealing with a large program, first estimate how many substantially independent elements will interact with each other in your program. Regardless of the level of organization, the fact that probabilities for independent events multiply tells you how many defects your software architecture can tolerate. Ten modules, each having a 99% probability of success (zero defects), have only a 90% probability of operating successfully when taken together ($0.99^{10}=0.90$). One hundred such modules operating together have only a 37% probability of success ($0.99^{100}=0.37$). You can keep quality high by either organizing

## Tools of the big-program trade

Million-line programs call for the same edit/compile/debug cycle as small programs do. But big programs call for so many passes through the cycle that you'll want to use software that streamlines the process. You'll also want software tools for tasks that you'd perform by hand for smaller programs. A list of such handy tools includes requirements-tracking tools; code browsers and understanding tools; configuration-management tools; check-in, check-out systems; make or build tools; and combinations of the above.

Requirements-tracking tools help you put specifications in manageable form and see that your team implements them. Code browsers and understanding tools search your code for a specific category of information such as names of classes or functions, caller/called-by information, or variables by type. The tools also produce graphic calling-tree displays, and some also assign complexity metrics to the resulting structure.

Configuration-management tools help you group and organize your programming teams, specifications, tools, or product. They can track relationships between subcomponents and differences between versions. Check-in/check-out systems simplify version tracking by coordinating access to documents by multiple team members working in close succession on the same documents. Make or build tools help maintain the programs that compile, order, and link the thousands of modules that make up a complete program.

Require from Paramax Systems Corp is a typical requirements-tracking tool. The tool lets you identify, analyze, and extract contractual requirements from any text, such as proposals and specification documents. You can then use the tool to allocate the requirements to other proposals, organizations, work-breakdown structures, or hardware or software items.

The tool traces one-to-many and many-to-one relationships between requirements and source documents. It also tracks parent and child relationships between requirements. The tool can link the text-based requirements it tracks to diagrams from CASE tools such as Software Through Pictures from Interactive Development Environments (San Francisco, CA) and Teamwork from Cadre Technologies Inc (Providence, RI).

Require runs on Unix workstations and costs $20,000 for the first seat and $7000 per additional concurrent user. Requirements and Traceability Management from Marconi Systems Technology (Chantilly, VA) is a similar tracking tool and also starts at $20,000.

An example of a tool set that can cut short the edit/compile/debug cycle is C++ Softbench 3.0 from Hewlett-Packard's Software Engineering Systems Div. This version of the tool makes C++ 3.0 easier to use by giving you tools for templates, nested classes, and exception handling.

tests to make the quality of the modules very high or by creating a hierarchy of tests to help integrate the base modules.

Software, or source lines of code (SLOC), is not, by itself, a reliable means of classifying small, moderately large, and really big programs. A first example of what can break the SLOC metric is a small team using GUI development tools and templating tools. That team can generate a large number of lines of code that do not, by themselves, constitute a "really big" program. A second case in which SLOC count hides complexity is control applications. These programs use many interacting functions, which rapidly increases complexity. How you define what comprises one program also affects the SLOC count. You may or may not refer to software running on a network of computers as one program, depending on the quantity, importance, and frequency of communications between the computers.

**The distributed software architecture developed by Paramax Systems Corp for the Canadian Patrol Frigate runs on 32 computers. The software, written in a decades-old standard US Navy language, operates all ship weapons automatically and reconfigures itself after battle damage to run on the available hardware.**

(One point we'll overlook when judging the size of programs is the language of the source code. In this report, we'll assume that the language is a third-generation one like

The base product includes three graphical browsers: The static graph browser shows relationships among program variables, functions, and C++ classes; the dependency graph browser gives graphical views of the structure of program makefiles; and the data graph browser displays a program's data structures. Additional features include a file compare and combine tool, an incremental linker, a Motif interface to the *vi* and *emacs* editors, and integrated version-control/configuration management. The tool set interfaces to HP or Sun compilers and debuggers and costs $4500 for the HP9000 or Sun SPARCstation.

Additional modules for C++ Softbench 3.0 give you tools for developing classes (C++ Developer, $2500), managing change requests (Changevision, $5950), developing methodologies (Synervision, $3950), and building other programs into the tool set (Encapsulator, $5000).

The class-development tool automatically generates source code, has dialog boxes for setting attributes of class-member functions, checks coding and design rules, and lets you graphically edit class inheritance. The change-request tool helps you define a set of tasks that include identifying and verifying defects, fixing and testing corrected code, and communicating status to other team members by automatically generating email. The methodology-development tool helps you define a generalized set of tasks according to the software packages involved, the tasks' priorities, and the standards, measurements, and reports needed at each stage.

Another tool set that improves work-group efficiency is Teamware from SunPro, an operating unit of Sun Microsystems Inc. Sun initially developed the tool set for internal use on the Solaris operating-system project, then refined and packaged it for commercial release. The Solaris team of 200 developers, organized in groups of 5 to 10 people, used the tool set to cope with 12,000 source files spread over seven buildings in three cities.

The tool set includes Versiontool—for visually inspecting and managing multiple versions of source files; CheckPoint—for capturing project source-file configurations for later retrieval; CodeManager—for graphically integrating and managing project releases; FileMerge—for visually merging source files and coordinating concurrent source-file changes; and ParallelMake—for building project components in parallel. The tool set's features position it between Unix utilities such as *sccs* and *rcs* and powerful, but complex configuration-management systems. Teamware is available for SPARCstations and 80x86 systems running Solaris and costs $995.

C or Ada, not assembler or a higher-level script. See **box,** "Ada and C++: differing strengths for large programs," for a discussion of how these two languages suit large programs.)

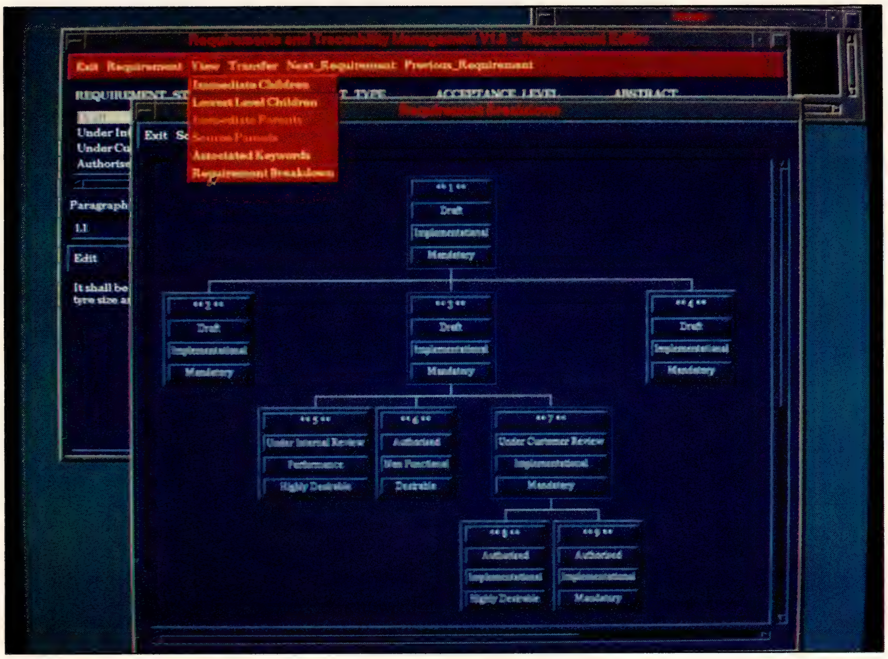
Many PC-based CAE tools belong to the lower end of the big-program spectrum. One such program is TangoPRO 1.0 from Accel Technologies Inc (San Diego, CA), scheduled for full release this month. This 32-bit pc-board design package runs under Windows and weighs in at about a million lines of code.

Jerry Burwell, vice president of engineering, headed the team that replaced the earlier DOS version of Tango with an object-oriented one written in C++. He started development with a team of 4 that increased to 12 and averaged 6 over the two years of development. The team used CASE tools at the beginning stages for analyzing and specifying the system and developing the software architecture. The team dropped the tools at the design stage when elaborating and updating the documents became cumbersome.

The team wrote functional specifications and design documents, did design reviews and code walkthroughs, and held peer reviews. Larger teams usually perform these tasks. The fact that this small team included them in its design process indicates a commitment to producing quality software. Each module and class included built-in self-tests, but Burwell reports that the overall code quality still depended on the determination and discipline of individual team members. Using C++ and developing test code paid off in fewer defects at the module level. Developing a hierarchy of tests to confirm module integration proved too time consuming, so the team relied on weekly "manual" builds.

A similar report on managing the complexity of multimillion-line programs comes from Aki Fujimura, vice president of central engineering and information services at Cadence Design Systems Inc (San Jose, CA). A vendor of workstation-based CAE tools, Cadence has over 10 million lines of code in its product line and more than 600 people doing development work. Fujimura's recipe for a very large CAE tool project is 3 to 4 million lines of code and a technical team of about 50 people. At Cadence, most engineering development teams consist of either 5 to 6 people or about 20.

Although Fujimura purchases software engineering tools for Cadence, he doesn't consider the tools to be as important to a big program's success as the project team's methodology and training. He considers using an explicit development process to be much more important than exactly which one you choose. An explicit process description gives the team common terminology so members can talk easily to each other about their work. (Cadence uses the process model devised by Watts Humphrey of Carnegie Mellon's Software Engineering Institute (Pittsburgh, PA).)



**As the number of requirements on large government programs climbs to the tens of thousands, tracking these requirements through to fulfillment becomes a large project in its own right. Two tools can help you trace relationships among requirements and between requirements and downstream management and technical documentation. They are the Requirements and Traceability Management tool from Marconi Systems Technology (shown) and Require from Paramax Systems Corp.**

Cadence uses configuration-management, bug- and code-tracking, and metrics-collection tools. The vendor develops most of these tools in house by using scripts to drive public-domain Unix utilities. Fujimura is waiting for the software-tools industry to develop metrics-collection tools that record, on a project basis, how long developers spend using particular tools and on what sort of tasks. Such metrics will serve as a basis for improving the big-program development tools and the ways that developers use them. He also points out that current CASE tools guarantee a certain minimum quality of work done by the least experienced programmers but hold back the experienced, leading-edge developer. He looks for development tools with abundant user-configuration options so his most experienced people can keep improving the tools themselves.

A third example of a million-line program comes from the government sector: the software system for the recently completed Canadian Patrol Frigate (CPF). Paramax Systems Canada, an operating unit of Paramax Systems Corp, developed the software. According to Richard Simon, vice president of engineering at Paramax Systems Canada, "CPF was the first surface combatant to use a distributed system integrated from sensors to weapons and with reliability and survivability built in."

Thanks to the high degree of automation made possible largely by its advanced software, the CPF's crew of 225 performs tasks similar to those that required a crew of 330 on a previous warship.

## Ada and C++: differing strengths for large programs

Coding a large program is a complex project that demands more services from a compiler than smaller programs do. Ada and C++ both supply some of these higher-order services including extensive type-checking, templating, and aids for writing code in modules and organizing large programs.

The first question to ask when comparing Ada with C++ is "Which Ada and which C++?" Although fairly new, both languages are poised on the brink of changes in the state of the art. The current ANSI versions of C++ are 2.0 and 3.0. The anticipated 4.0 version will add exception-handling and re-standardize features, such as templates, that now differ from vendor to vendor. The current version of Ada has been around since 1983. The next five years will see a transition to the new 9X version.

The current version of Ada is easy to read but is more extensive than C++. Ada costs you time when writing programs, but gives it back in relatively easy debugging. On the object-oriented front, Ada includes encapsulation, and polymorphism will come with version 9X. Ada already has a reputation as a good language for big systems, as it should: The US Department of Defense had it designed for that purpose.

Ada's program library is especially useful for large programs. The program library is a compiler-generated description of a program. It consists of packages, which are units of code that group related parts of a program—subprograms, types, variables, constants—in one logical unit. The program library lessens the need for global names because packages reduce name conflicts.

Ada 9X is moving toward a true hierarchical name space for global names. This naming convention will be roughly analogous to Unix or VMS file systems, which are akin to trees of directories. Features that see common use by convention now will become standard in the new versions of both C++ and Ada.

C is notoriously unreadable. C++ includes all of C, plus extensions. The C++ extensions are still visually dense because of the abundance of special characters and multiple interpretations of keywords such as *virtual* and *static*. Knowing C gives the experienced programmer a leg up on learning C++. But once you know both C++ and Ada, you'll find it easier to write code in C++ and easier to debug code in Ada.

C++ lets you do object-oriented programming, whose hallmarks are inheritance, encapsulation, and polymorphism. The C++ class is a less-capable unit of code than Ada's packages. C++ currently has a single global space at the top-level block and a single class-name space.

Ada has strong and extensive type checking. In Ada, every name has its own type. Ada does runtime checks for array bounds and pointer mistyping and reports errors as runtime exceptions. Debugging in Ada is much simpler than debugging in C++ because runtime errors are identified by line location. New York University (New York, NY) offers a free Ada interpreter and is developing a free compiler for release in 1994.

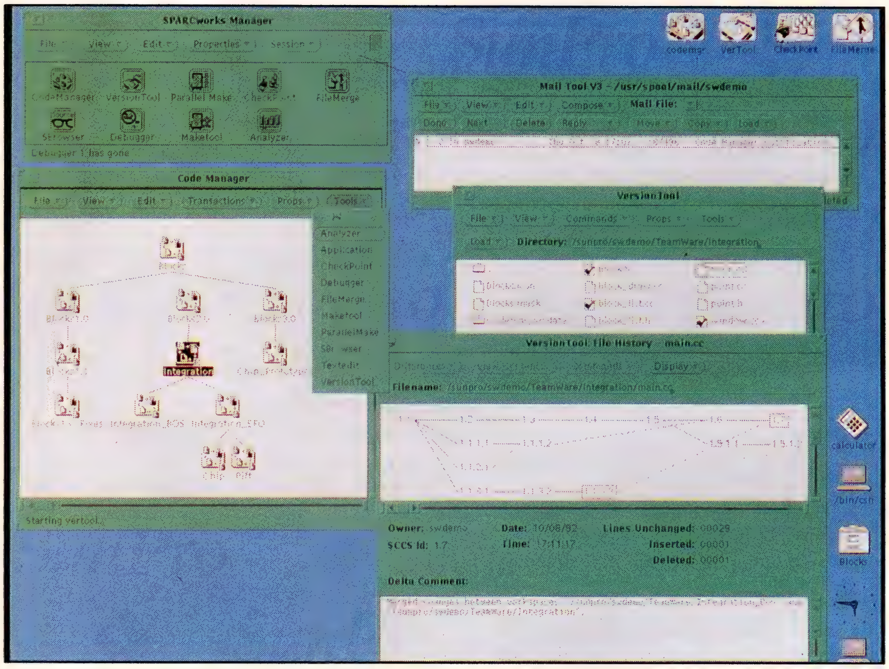
C++ type checking is fairly strong, but the language does not check multiple pointers to the same type or user-defined arrays. You can freely cast pointers to integers in C++, and the compiler itself does lots of type conversion. As a result, you catch fewer errors at compile time. C++ detects array bounds and pointer mistyping only when some downstream part of the program gets trashed, which can be millions of operations later. C++ is a popular language, and much training material is available compared with the more limited Ada market. The Free Software Foundation offers a free C++ compiler.

Ada and C++ are coming together in speed and in size of the executable and development environment. The two run at similar speeds if you turn off the Ada runtime checks, and C++ compilers are getting to be about as big as Ada ones. The speed penalty imposed by runtime checking ranges from 10 to 50% for both languages, depending on how you write the code.

The current trend in C++ development tools is to add Ada-like checking. Examples of such tools are Softbench from Hewlett-Packard and Objectcenter from Centerline. In general, language designers shoot for consistency by solving problems such as runtime type-checking themselves instead of leaving the corrections to a patchwork of add-on tools.

For example, in automatic mode the combat system takes over nearly all the functions of the human operator. The system then detects and fires weapons on multiple submarines, aircraft, antiship missiles, and surface vessels, as required.

A redundant serial data bus ties all the ship's sensors, weapons, computers, and displays together. The bus' software includes 146 program modules. The ship can tolerate moderate battle damage without a serious lapse in performance because the distributed system architecture can automatically reconfigure itself and reassign functions among its 32 computers and 18 operator consoles. For example, battle damage that switches off the anti-air-warfare computer can cause the anti-submarine-warfare computer to take over transparently.



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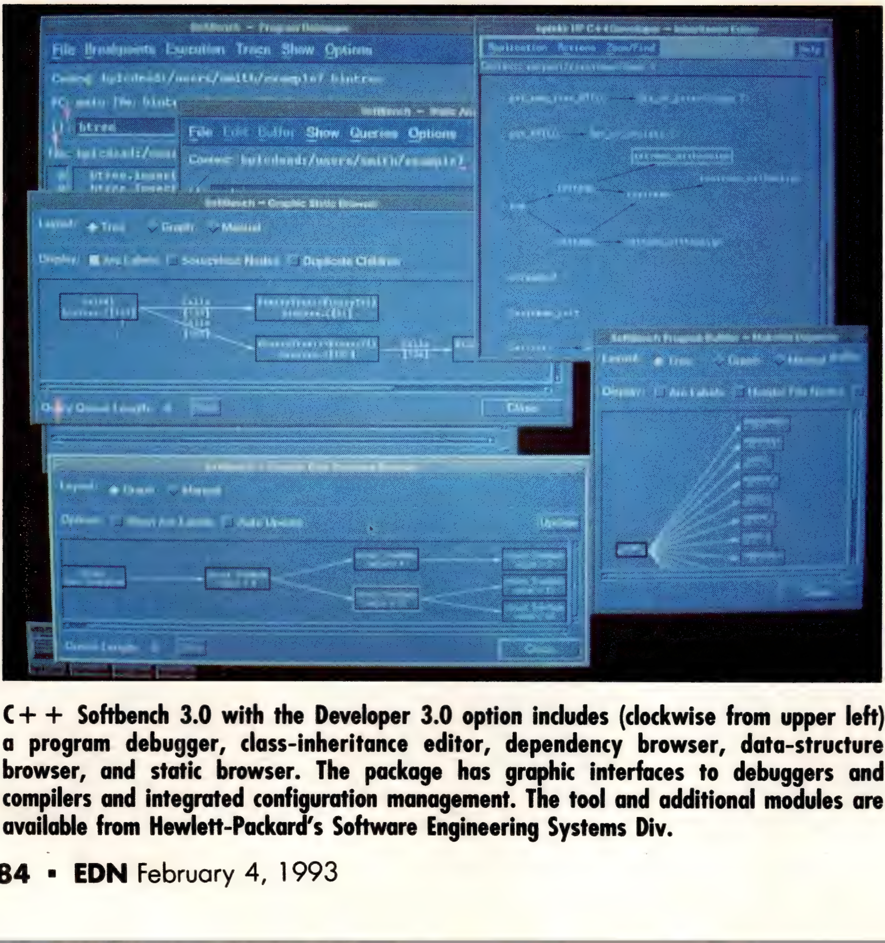
**Teamware from SunPro includes a tool manager, Parallel Make, code manager, version tool, mail tool, and (icons) Filemerge and CheckPoint configuration tool.**

Large government systems such as the CPF system often represent unique advances in engineering's state of the art but also face unique problems. The systems tend to be long-lived, enduring for decades. Their development cycle should allow for long and thorough front-end planning. Practical budgeting will recognize and fund this long amortization period.

As with many large projects, the customer—in this case the government—is a very large organization. Development may follow a phase of technical experimentation, but development is far from a sure thing—it's also an experiment. The experiment is that of developing project teams from the customer and software-developer organizations. Just reaching a consensus on the software requirements is much of the battle toward building the system. With the requirements count reaching 20,000 to 50,000, dedicated software tools become necessary for tracking requirements from the beginning to the end of the project. Government customers also fight to deal with the great diversity of their systems and impose the resulting controls on the software-development team. A development procedure that works for a large project can bury a small one with unnecessary organizational structure and control.

When large organizations work on large enough projects, they'll



**C++ Softbench 3.0 with the Developer 3.0 option includes (clockwise from upper left) a program debugger, class-inheritance editor, dependency browser, data-structure browser, and static browser. The package has graphic interfaces to debuggers and compilers and integrated configuration management. The tool and additional modules are available from Hewlett-Packard's Software Engineering Systems Div.**

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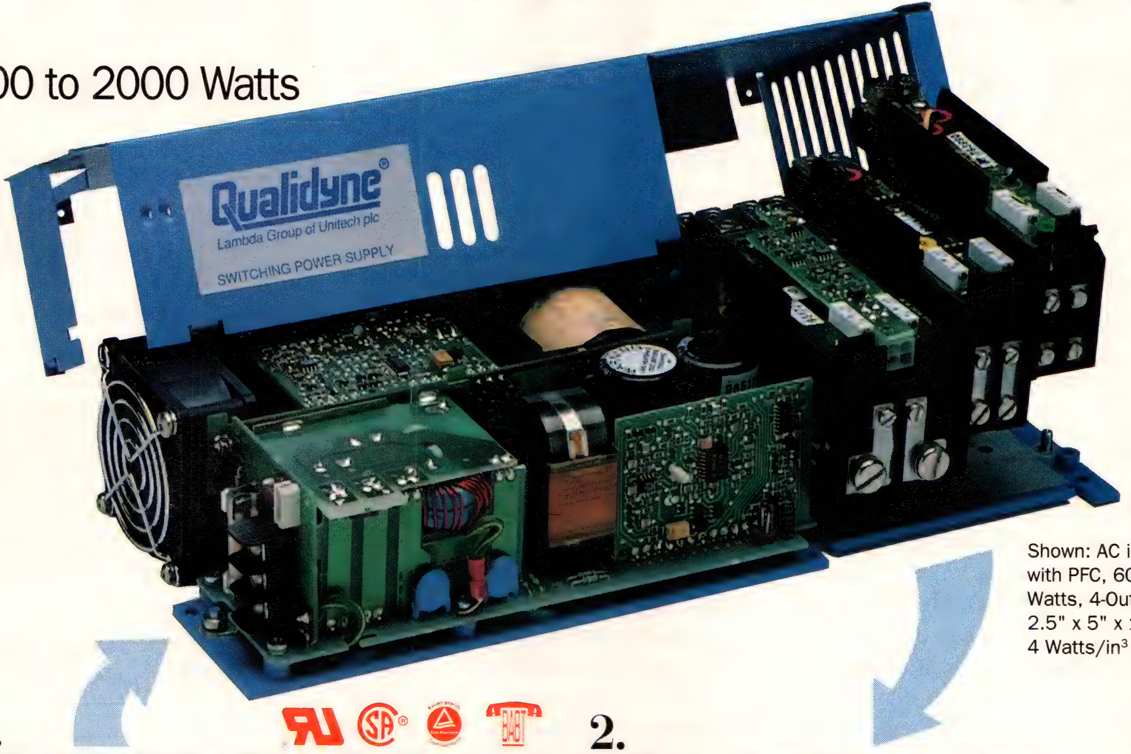

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Qualidyne Systems, Inc. • 3055 Del Sol Boulevard, San Diego, CA 92154 • Tel: (619) 575-1100, Fax: (619) 575-7185 write their own languages, such as the US Navy's decades-old CMS-2. The CPF used it, and it was the Navy's standard language before the recent Ada mandate. Paramax still writes programs in CMS-2 for existing projects and for new projects that use pieces of old code. The company also re-engineers CMS-2 into Ada. Developers translate some code by hand and use internally developed translation tools.

Newly written lines of code for a next-generation large passenger plane, the Boeing 777, will amount to around one million lines, according to Keith Hill, who manages the project at Boeing Commercial Airplane Group (Seattle, WA). Flight tests are to begin in mid 1994, and the project is now at the critical integration phase of development. Design and coding is complete for the long-lead modules and has just begun on the shortest-lead modules.

Like most large projects, this one is a mix of internally developed code (about 20%), subcontracted code, and reused or rewritten code. Software runs the plane and operates as an integrated system that reaches into all aspects of its operation. About the only software that does not connect to the system is the program that controls the cooking equipment in the galley.

The plane controls are fly-by-wire with 9 times redundancy and one pneumatic backup. The redundancy consists of three parallel channels of control. Each channel has three architecturally dissimilar processors all running software to the same specification. The software architecture relies on two types of high-speed data buses. The first is an Ethernet-like bus used mostly in the passenger cabin. This bus handles tasks such as maintaining the passenger and gate lists for each landing and has a low integrity requirement. The second bus meets ARINC629, a Boeing-originated standard for high-integrity data.

Ada is the designated language for the 777. There are 35 Ada hardware boxes on the 777, up from 4 in the 777's predecessor, the 747400. Using commercial off-the-shelf C software forced C on some boxes to maintain a single language on the box. The need for speed forced assembly language on a few other boxes. Because subcontractors are developing most of the software for the 777, the choice of software engineering tools lies with them. Boeing developed their main source-code analysis tool in house and also uses an off-the-shelf C analysis tool.

**Acknowledgment**

*Thanks go to Chief Scientist Tucker Taft, Ada Div of Development Systems Group, Intermetrics Microsystems Software Inc (Cambridge, MA), for information about Ada and C++.*

*Technical Editor John C Napier can be reached at (617) 558-4690; FAX (617) 558-4470.*

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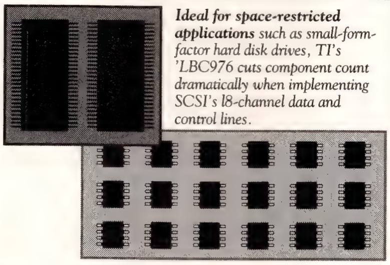

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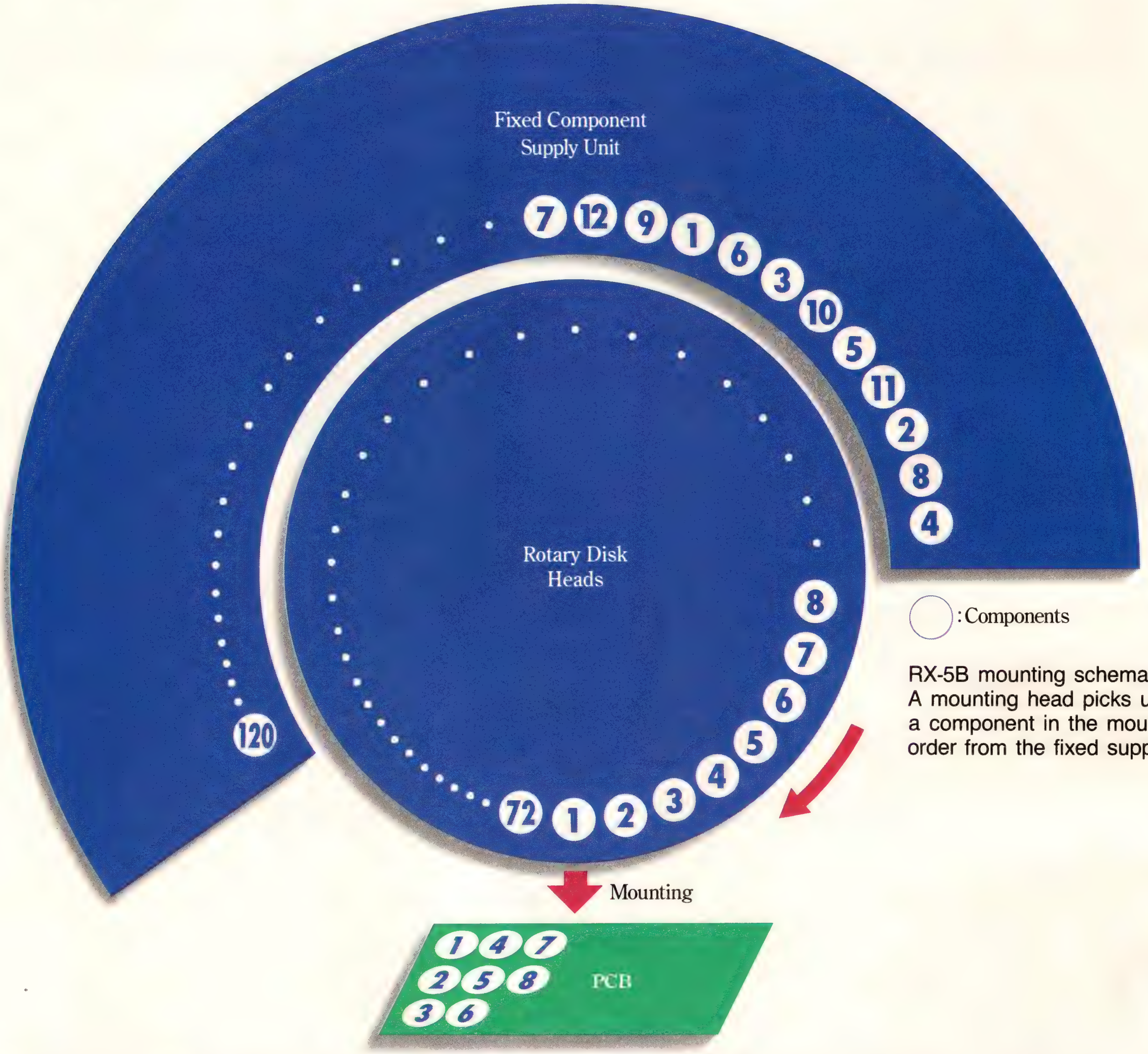

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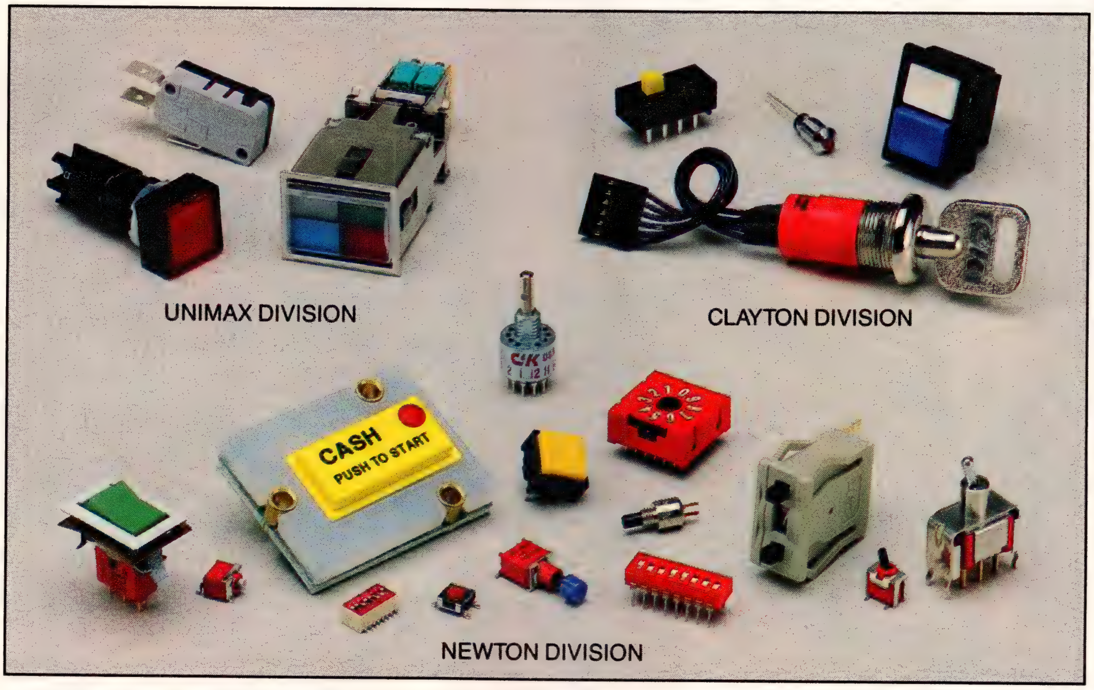

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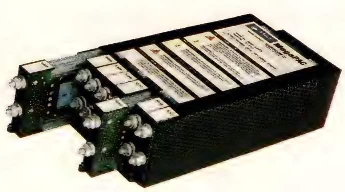

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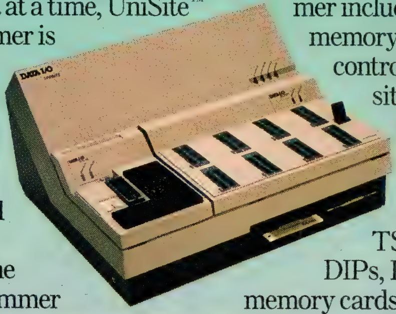

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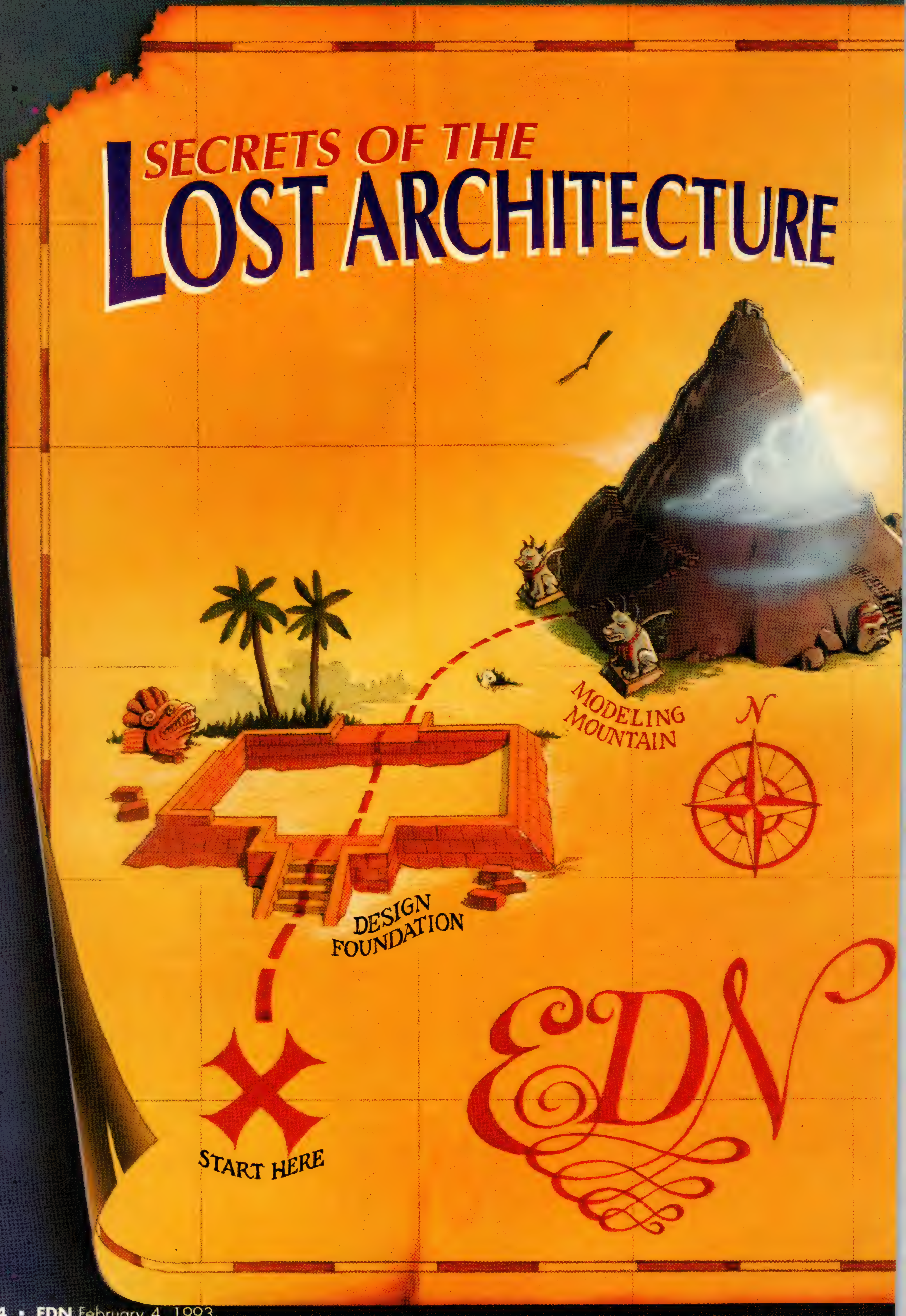
CIRCLE NO. 68

# SECRETS OF THE LOST ARCHITECTURE



### EDN HANDS-ON VHDL DESIGN PROJECT—PART 3

# Writing the Code

**MICHAEL C MARKOWITZ, Editor EDN Asia**

In the first two installments of this series, I assembled EDN's design center and made it operational. I also chose a design—the Z80—and zeroed in on a strategy for modeling it. After performing all this preliminary work, I was ready to begin creating, writing, and debugging the model.

Before I started to write the model code on the HP/Apollo DN4500, I did some work with paper and pencil. First I created a register map. The register map included all of the processor's directly addressable registers as well as those not directly accessible to the user. The registers included eighteen 8-bit data registers; four 16-bit registers for the program counter, stack pointer, and two index registers; data and address latches; and 1- and 2-bit-wide registers for interrupt-

Illustrations by Bob Doucet

## Writing the Code

enable and interrupt-mode storage.

After creating the register map, I set to work on the processor's two main state machines. The first state machine is a relatively small one that controls the CPU during a reset operation **(Fig 1)**. Contrary to conservative design practice, the Z80's designers didn't use the hardware reset to clear all storage elements. According to the Z80 specification, $\overline{\text{RESET}}$ initializes the CPU by resetting the interrupt-enable flip-flop, clearing the program counter and interrupt and refresh registers, and setting the interrupt status to Mode 0. In addition, a reset forces the address and data bus to a high-impedance state, and all control signals become inactive. Finally, the specification insists that $\overline{\text{RESET}}$ must be active for a minimum of three clock cycles before the reset operation is complete. I took the 3-clock-cycle requirement to indicate—and Zilog later confirmed—that the Z80 uses a synchronous reset rather than an asynchronous one. As a result, I wrote the state machine to transition on rising clock edges and the internal reset signal to go active on the third rising edge after $\overline{\text{RESET}}$ goes low.

Although designing the reset state machine was straightforward, it immediately illustrated to me the difference between doing the design as a hardware designer and programming the design as an HDL programmer. According to the specification, when the $\overline{\text{RESET}}$ line is forced low, the IC waits three clock cycles before accepting the reset. A hardware designer would add a 3-stage shift register to create this 3-cycle delay, but the software solution is to use a counter. The EDN model counts three clock cycles, resets the appropriate registers, then stalls until $\overline{\text{RESET}}$ goes inactive. After $\overline{\text{RESET}}$ goes high, the model stalls for two more clock cycles before resuming normal processing (**Listing 1**). After developing the reset process, I then created a state machine for the bus arbitrator based on the bus-arbitrator state diagram **(Fig 2)**.

I was careful to document the code as I wrote it. Theoretically, the documentation would allow me—or anyone else reading the code—to figure out what my intent was and what the software model was trying to accomplish in a particular section of code. Some modelers recommend that one-third to one-half of the writing in a complex model be comments that describe the model's operation. The Std_ModelSpec section of the Std_DevelopersKit recommends that comments should account for roughly 20%. Std-ModelSpec also suggests that among the important comments to include are those that explain the limitations of your VHDL usage and those that identify assumptions you've made in developing your model.

Although I attempted to document EDN's model thoroughly, my comments helped little when, months later, I attempted to decipher the model I had written—and they were virtually worthless to others reading the code. Documenting code presents several problems. First, rather than explaining an entire block of code, the comments tend toward documenting too small a function. In addition, often the coder (and documenter) knows his intent too well and underestimates the need for explanation. One software-documentation problem I'd heard about was that programmers—like lawyers—have their own language that is incomprehensible to hardware designers (witness the *VHDL Language Reference Manual*, **Ref 1**).

I considered embedding the reset state machine inside the bus-arbitration state machine. Ultimately,

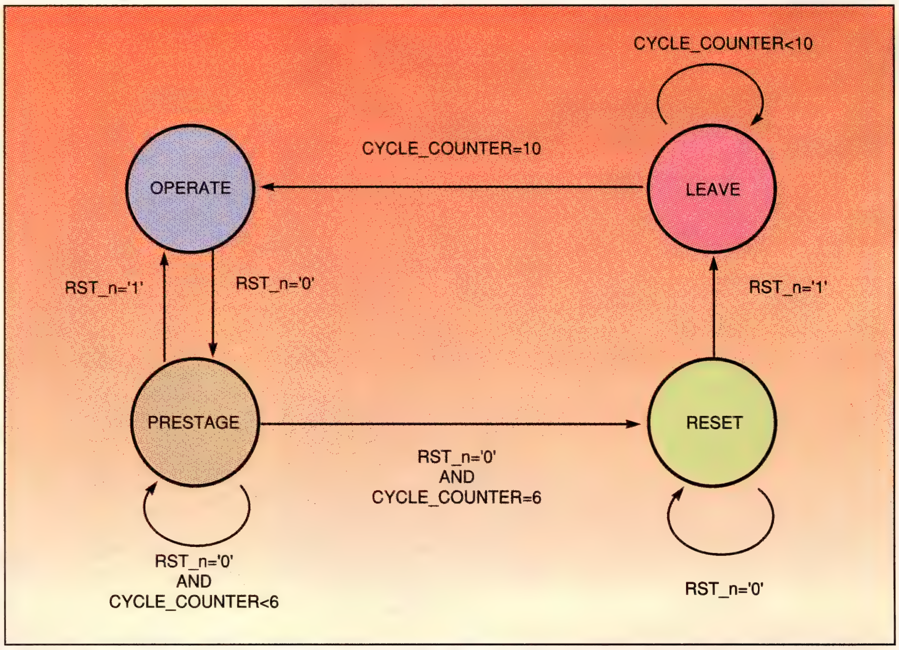


**Fig 1—The state machine for the reset logic is a simple machine that transitions between its four states depending on the values of RST_n and cycle_counter.**

I decided to keep the two machines distinct because of the 3-cycle minimum pulse-width specification of the reset signal. If the reset machine were embedded in the bus arbitrator, a short pulse would disorient the bus arbitrator. As a separate process, the arbitrator can continue operating until three clock cycles validate the reset signal.

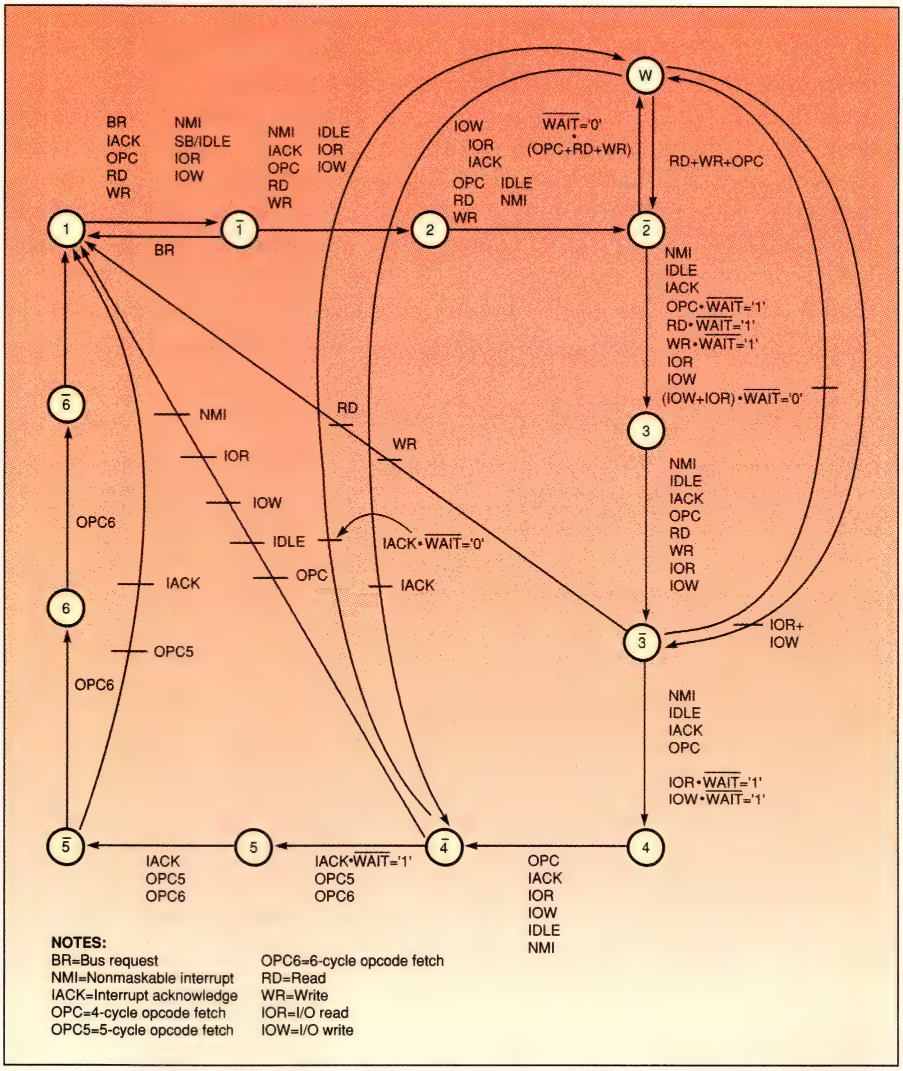
**A compiler is the greatest syntax checker in the world and it costs the same whether your code is messy or clean. Use it early and often to check that your syntax is correct.**

One mistake that I made constantly was using single and double quote marks incorrectly. Although I was sure there was a standard scheme, my failure to identify it led to numerous compiler errors. VHDL uses quote marks to enclose characters and strings. Simply, and correctly, characters, such as '1' and '0', are enclosed in single quotes; strings, such as "10010000," are enclosed in double quotes.

The bus-arbitrator state machine presented its own problem. The machine operates on both edges of the clock. Unfortunately, Synopsys' synthesis software has a strict syntax for edge-triggered flip-flops, which prevents you from synthesizing logic that changes state on either clock edge in a single VHDL process. I decided that I would generate, by synthesis if possible or by hand if not, a frequency doubler that would double the input clock and allow the internal circuits to operate off the 2× clock. I could also have split the design into a positive-edge triggered process and a negative-edge triggered process, though coordinating signals between the two processes would have added complications. Whether the internal circuits operate off the rising clock edge of a 2× clock or off both clock edges on a normal-speed clock doesn't change the internal circuit operating requirements or the external interface requirements, so the adjustment was benign.

Aside from the 2× clock, the bus arbitrator was mostly straightforward. I could have written the state machine using a CASE statement or an IF, THEN, ELSE. Both constructs synthesize into a decoder structure, though the case builds a multiplexer-based decoder. In contrast, the IF, THEN, ELSE builds a priority decoder. If your decoder is fully specified, then you can use the constructs interchangeably.

If you don't decode several states, then the IF, THEN, ELSE will use logic more efficiently because it won't decode the unused states. In contrast, VHDL requires that you lump all unused CASEs into a WHEN OTHERS clause, creating extra logic and a less-efficient decoder. CASE constructs simulate faster than IF, THEN, ELSEs, however, because they don't need to test IF conditions sequentially. The EDN bus arbitrator was fully specified, so I used a CASE for faster simulation.


W
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5
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BR IACK OPC RD WR
NMI SB/IDLE IOR IOW
NMI IACK OPC RD WR
IDLE IOR IOW
BR
IOW IOR IACK
OPC IDLE RD NMI WR
$\overline{WAIT}$='0' • (OPC+RD+WR)
RD+WR+OPC
NMI IDLE IACK OPC•$\overline{WAIT}$='1' RD•$\overline{WAIT}$='1' WR•$\overline{WAIT}$='1' IOR IOW (IOW+IOR)•$\overline{WAIT}$='0'
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NMI IDLE IACK OPC IOR•$\overline{WAIT}$='1' IOW•$\overline{WAIT}$='1'
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OPC6
OPC5
OPC6
OPC IACK IOR IOW IDLE NMI
IACK•$\overline{WAIT}$='1' OPC5 OPC6
IACK OPC5 OPC6
NOTES:
BR=Bus request
NMI=Nonmaskable interrupt
IACK=Interrupt acknowledge
OPC=4-cycle opcode fetch
OPC5=5-cycle opcode fetch
OPC6=6-cycle opcode fetch
RD=Read
WR=Write
IOR=I/O read
IOW=I/O write

Fig 2—The bus-arbitration state machine had 13 states to track and 10 different modes (operations) in which to transition between states. As a result, we had to develop a shorthand notation to keep track of the output conditions that resulted from each of the state transitions.

## Writing the Code

**When you battle against an opponent, surprise is a strategic part of your arsenal. In circuit design, you are competing against yourself. To prevent surprises, design your circuits in small pieces and verify each piece before moving on.**

After writing the VHDL code for the state machines, I needed to test their operation. All of the VHDL intelligencia recommend "going deep before going wide." This expression suggests that rather than designing your entire circuit in a single pass before testing it, using VHDL or any other technique, you should test each piece as you build it. The technique offers several advantages. First, it ensures that each module of your design is—at least to the extent that your test program checks—properly functioning. Second, as you find your mistakes, you can correct them before you replicate them throughout your design. Third, and perhaps most important, when you do encounter problems integrating all of the pieces, having tested each one individually helps you localize design flaws. Steve Carlson, ASIC R&D program manager at Synopsys, suggested that I go beyond verifying the correct function of the modules. He recommended that I also synthesize the blocks.

In the beginning, it was easy to test and synthesize the circuit; there wasn't much to it. As the design grew, it became more and more unwieldy to verify. In fact, before long, I stopped verifying functions and stopped running the synthesis tools on the growing design. Instead, I concentrated strictly on writing the model. Testing and debugging the pieces of the model was too much work and offered too little reward. Each functional block had too many inputs and outputs, figuring out test patterns to test the blocks comprehensively was not trivial, and writing the test benches to perform the tests would require a substantial amount of time. I therefore defied conventional wisdom and postponed test and debug until all of the pieces were written and assembled.

Following the bus arbitrator, my next task was to write the instruction decoder. This chunk of logic reads the 8-bit instruction and decides, first, what operations the CPU will perform on what pieces of data and, second, in what sequence to perform these operations. Zilog's *Z80 CPU Technical Manual* (**Ref 2**) told me the sequence of op-

## Helpful tools take time

Several tools were available to assist me with writing VHDL (VHSIC hardware description language) code. Vista Technologies (Schaumburg, IL) offers a set of syntax checkers and templates that guide your development efforts and minimize the likelihood of language-based errors. Developers wishing to avoid writing code also have several choices. Lewis Systems (Irving, TX) developed a tool that accepts signal relationships as inputs to a spreadsheet. The software converts the relationships to VHDL and generates all of the necessary peripheral code to define signal and variable types, as well as function and procedure calls. State-machine-based designs can use software from iLogix (Burlington, MA) that converts state diagrams into VHDL.

I ultimately chose not to use any of these tools for several reasons. First, I was concerned about getting caught up in the sexiness of the tools. Although every tool looks beautiful in a demo, each has its own strengths and weaknesses, and you don't find either without extensive experimentation. I didn't feel I could devote enough time to this evaluation. Despite my decision, the Vista tool would have been invaluable for eliminating the incomplete or confusing error messages that came up during the model analysis whenever the VHDL analyzer encountered missing or improper syntax.

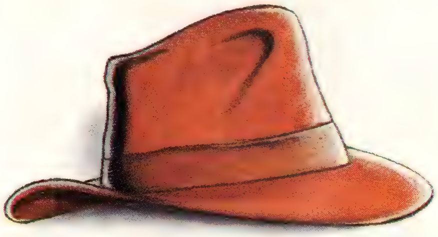
Second, some of the tools weren't consistent with my vision of how I wanted to perform the design. Initially, I intended to write one model that I could simulate and synthesize. The Lewis Systems and iLogix software packages both could generate simulatable VHDL. However, although both companies were working with synthesis vendors to close the gap, neither promised synthesizable code.

Fortunately, model development is clearly heading toward graphical-entry techniques. Better still, these graphical-entry tools are considering synthesis. Since I began the design, several companies have introduced specialized graphical-entry software. Among these companies are Viewlogic (Marlboro, MA), Comdisco Systems (Foster City, CA), Fela Speed (Neuchatel, Switzerland), and Synopsys (Mountain View, CA). Software packages from each of these companies generate synthesizable VHDL from graphical representations of portions of your design.

erations that each instruction performs. The manual breaks instruction cycles into one or more operation or "machine" cycles. These machine cycles include instruction fetch, memory read and write, input and output, and bus request and acknowledge, among others. Each machine cycle is further divided into two to seven T cycles, which is the number of clock cycles each machine cycle takes to execute.

The technical manual provides such details as the opcode that causes the CPU to execute an instruction, a description of the instruction, the number of machine cycles the instruction requires to execute, and the status flags the instruction affects. As an example, the ADD A,n instruction causes the CPU to add the value n to the value in register A—also called the accumulator—and store the result in the same register. The instruction requires two M cycles to execute. The first M cycle, an instruction fetch, is four T cycles. The technical manual tells you that the second M cycle takes three T cycles. The manual leaves it to you to infer that this M cycle is a memory read. The read allows the CPU to read the immediate operand for the addition operation.

Although the manual provides similar information for each of the Z80's instructions, on several occasions I found the information in error. Fortunately, Zilog bailed me out. The company maintains a document that describes each instruction's byte length and its number and sequence of machine cycles. I used the document to fill in some of the gaps, but it, too, was not perfectly accurate.



You can write an instruction decoder in several ways. You can explicitly decode every one of the possible 64k 2-byte opcodes—of which less than 512 are actually used; you can explicitly decode just the opcodes used; or you can utilize patterns in the opcodes to reduce the opcodes to a reasonable number. I carefully examined the opcodes for patterns that would allow my decoder to consolidate the number of explicit opcode references. Still, the EDN model's decoder recognized and accounted for several features of the Z80 that complicated construction of the decoder. Among these features were 1- or 2-byte instructions, operations involving the index registers, and operations involving the index register where the actual instruction isn't read until the fourth clock cycle of the instruction.

The instruction decoder is large and has several levels of decoding. Even before it evaluates the particular instruction, the decoder considers whether the instruction is the first or second byte of a single- or multiple-byte instruction. If the opcode is the second byte of the instruction, flags set on the first pass through the decoder guide the opcode to the appropriate decode structure. As I did with the bus-arbitrator state machine, I implemented this decoder mostly with CASE constructs. My reasoning was similar. Fully specified decoders simulate faster as CASE statements than as IF, THEN, ELSE at no additional cost in logic.

Although Zilog supplied me with the length of all instructions, I stumbled over some of them. For

## How good is your model?

Models are similar to snowflakes in that no two are alike—even if they meet the same specifications. For this reason, while a model may be bad if it doesn't meet its function and performance criteria, deciding whether the model is good is far more difficult. In fact, all of the criteria for evaluating a model's goodness are relative. Counting the number of lines of code in a model, for example, is a useful measure of the relative efficiencies of two models for the same function, but how many lines of code should the function require? Among the relative criteria you can use to benchmark a model are

1) Is the model efficiently coded?
2) Does the model simulate well?
3) Does the model synthesize well?
4) Is the model easy to modify for corrections or additional features?
5) Is the code well documented and easy to follow?

Because there are no absolute measures of a model's goodness, we'd like to suggest an answer to your boss' inevitable question about the goodness of *your* model. Tell him it is the best model that has ever been written. In fact, tell him that your model is the one that all other models aspire toward.

**Be careful in singing the praises of your model. If you aren't humble enough, you may find yourself training and supervising a team of modelers.**

## Writing the Code

example, the Z80 instruction set includes several exchange instructions. EXX causes the CPU to exchange the data pointed to by the address stored in BC, DE, and HL with the data pointed to by the address stored in the alternate registers BC′, DE′, and HL′. What had me scratching my head was that the instruction apparently moved 96 bits of data across an 8-bit bus in one clock cycle. The obvious solution, as EDN's Executive Editor Steve Leibson pointed out, was that the data didn't move, but the register pointers did.

The final large block in the model was the execution unit. This function receives the decoded instruction from the decoder and ensures that the processor performs the appropriate operations for that instruction's execution. The implementation approach I chose was to group instructions that performed similar operations into a subprogram. For example, the EDN model initially grouped all logical operations, all arithmetic operations, all I/O operations, and all load operations.

In practice, the model ended up with several groups for some operations. For example, the Z80 offers 10 different addressing modes. I found putting all of these addressing modes into a single procedure made the procedure extremely large—not to mention difficult to test and maintain. As a result, I broke these large groups into smaller, more manageable ones. These smaller procedures were easier to visualize and therefore easier to debug.

Although the instruction decoder and execution units compose the skeleton, the subprograms were the meat of the CPU. In these sections, the CPU actually performed the work that caused data movement, manipulation, and management. The subprograms loaded registers with operands, updated the sequencer that guided the bus-arbitration state machine to its next state, and maintained the stack pointer and program counter. Ironi-

## Adding is easy

Since VHDL is strongly typed, when you try to add an integer to a bit_vector using the "+" operator, you'll generate a type mismatch. If you want to add data of these types, you must implement the addition operation by type-converting the bit_vector into an integer, by type-converting the integer into a bit_vector, or "overload" the addition operator. All of these approaches are relatively simple, though they generally involve adding a function to your model.

Where you perform this type conversion is largely a matter of style. For example, you can type-convert in the body of your code:

```
PC := PC + convert_to_bit_vector(1);
```

or

```
PC := convert_to_bit_vector
      (convert_to_integer(PC) + 1);
```

where convert_to_bit_vector and convert_to_integer are function calls that you've written for your model. You can put these function calls in the architecture—or better, in a package that the architecture references. By putting the function in a package, you make it accessible to other architectures.

Another approach is to perform the type conversion inside a package. To do this, you "overload" the "+" operator. The + operator gets its default meaning via a function definition in the package STD that comes with VHDL tools. This function definition requires that the inputs to the function be integers. When you define a similar function that uses the + operator but requires a bit_vector for one input and an integer for another, you have overloaded the + operator. The VHDL compiler will reference the appropriate function by matching the input types against the function's required types when it processes the code.

The overloading capability of VHDL and the language's strong typing argue in favor of naming generic functions with the same name. If you name all of your convert-to-integer functions "to_integer," then whether you need to convert a bit_vector, an enumerated type, or any other type to an integer—as long as you've overloaded the function with the appropriate elaboration—you don't have to remember any special name.

cally enough, these code fragments, constituting the greatest investment of time yet, were often easier to write than the skeleton.

In large measure, these subprograms were easy to write because their operation and function was obvious—and sequential. If you wanted to increment the program counter, you could write

```
PC := PC + 1;
```

which assumes that '+' is overloaded with a function that can add bit_vectors and integers and return bit_vectors (see **box**, "Adding is easy"). In contrast, some of the operation of the skeleton depended on signals and variables that were changed in different locations in the program. Signals were the most difficult to use. Although the value of variables can change in different parts of a process or in subprograms, concurrently executing processes can change signal values simultaneously. In practice, the danger of simultaneous processes forcing the same signal to different values was more of a conceptual problem.

**Don't try to use VHDL signals in multiple processes to drive the same signal unless the signals are 3-stateable. The signals are not democratic. They will contend for the wire.**

After falling into the trap several times, I realized that allowing signals to be driven in more than one process created the potential for contention. The reason is that VHDL creates a driver for each signal in a process. When you assign signal values to the same signal in more than one process, you have more than one driver. VHDL provides only one means for arbitrating among these multiple drivers: using resolved signals. These signals call a resolution function that you define in one of your packages. The function evaluates each of the drivers and assigns a new value. Unfortunately, the function rarely assigned the value I expected to the signal. Whereas I wanted the latest assignment to take precedence, the resolution function operated under the belief that both signals were contending. If the model had driven the $\overline{\text{READ}}$ low in one process, and then, in a later time interval, driven it high in another process, my aim was for the resulting signal value to be high. The contention forced the signal to the simulator value "unknown."

## Code efficiently

In many cases, fewer lines of code translate into better models. Bill Billowitch found several examples in the EDN Z80 code where I took a simple procedure and made it more difficult. My coding style may have reflected either ignorance of the language's capability or—more likely—an oversight of the obvious.

```
          Verbose                                 Concise
 IF (bit_1) = ’1’ ) THEN                    bit_2 := bit_1;
       bit_2 := ’1’ );
    ELSE
       bit_2 := ’0’ );
 END IF;
```

or

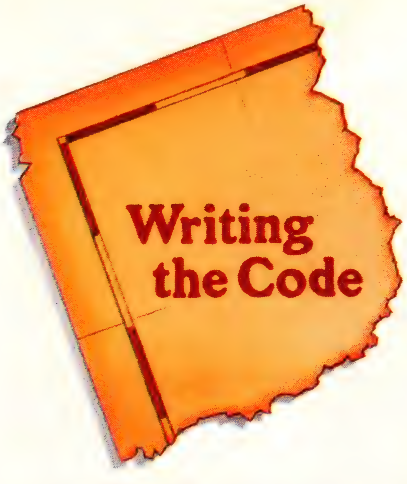
```
          Verbose                            Concise
IF (Boolean) THEN                  Boolean := NOT Boolean;
      Boolean := FALSE;
   ELSE
      Boolean := TRUE;
END IF:
```

Another example regards performing data-bit rotates:

```
flag(carry) := accumulator(7)
FOR i IN 7 DOWNTO 0 LOOP
   accumulator(i) := accumulator(i-1);
END LOOP;
accumulator(0) := flag(carry);
```

could be

```
flag(carry)  := accumulator(7);
accumulator(7 DOWNTO 1) := accumulator(6 DOWNTO 0);
accumulator(0) := flag(carry);
```



## Writing the Code

In reality, what the model needed was to remove the signal driver that had driven $\overline{\text{READ}}$ low in the earlier process. In effect, these signals are multiplexed on the same wire, so the model needed to force one driver to high impedance. Because I didn't always know, a priori, when to turn off a signal driver in a particular process, I found a different approach. The approach integrates multiplexers and handshaking to turn interprocess-communication signals on and off rather than directly driving signals in multiple processes.

Signals and variables presented another problem. At the outset of the design, I tried to keep separate functions in separate processes; I knew that doing so would make the model easier to synthesize. As I wrote the model, the problem of interprocess communication interrupted my progress. When you use signals as interprocess communicators, their value isn't updated until the end of the time delta. This time delta occurs after all of the sequential code in the process, and in concurrent processes, has executed. As a result, you can neither use the signal as an immediate branch-control mechanism in the same process, nor can you use the signal to communicate simultaneously with a concurrent process.

Consider an example. In the Z80 model, MACHINE_CYCLES is an enumerated type of all of the T states of the Z80. NEXT_STATE is a variable of MACHINE_CYCLES that tells the bus-control state machine, instruction decoder, and execution unit what T state the Z80 will go to next. During execution, depending on what operation the CPU is performing, NEXT_STATE could be assigned in any of the three function blocks (bus control, instruction decoder, or execution unit). If NEXT_STATE were a signal in three processes, there would need to be a mechanism to turn off the other two signals whenever the third tried to drive the signal; this mechanism doesn't exist. What the model needs is a more contorted mechanism for assigning and deassigning the signal. A less sticky problem is that the current model uses the NEXT_STATE variable as the new value for the variable BUS_STATE; you could move this assignment to the beginning of the process.

It wasn't until very late in the design that I had a revelation that might have saved me quite a lot of aggravation in dealing with this contention and coordination. Whenever I thought about coordinating multiple processes, I thought of a zipper metaphor—having the two (or more) processes trade signals in a coordinated fashion. Delayed signal assignments invalidated this concept. A simpler approach would have been to assign all of the signals to variables at the beginning of a process and all of the variables to signals at the conclusion. Instead of a zipper, this method is a conceptual loop.

Communication of another sort also presented a problem. In my first attempt at each instruction procedure, the model put addresses on the address bus and wrote to or read from the data bus depending on the instruction. This approach couldn't work. If you put an address on the address bus, you must wait for the memory access time before you read the data, otherwise the data is invalid. This realization forced me to use an intermediate register for the data and another for the address. Inside the instruction procedure, the model writes or reads information from these intermediate registers. The bus-arbitration procedure controls when these intermediate values are put on or read from the appropriate external buses.

While coding the model, I found that progress on some days was far better than on others. You should recognize that modeling is a concentration-intensive task. On some days, your concentration will be terrific, and you'll make excellent progress. On other days, your concentration will be awful, and you'll be better off going fishing.

**Writing a good model doesn't require that you think exclusively like a programmer. However, there are programmer tricks and techniques that you can adopt to speed and simplify the task.**

I also learned several tricks that programmers and code writers probably take for granted and that hardware designers might not fully appreciate. In my few past experiences with writing code, I invariably forgot to close an IF construct or a parenthesis. Poorly localized and often vague error messages, upon code compilation, forced me to perform line-by-line searches in an attempt to find the missing element. There is a better way.

First, Bill Billowitch of The VHDL Consulting Group instructed me to open and close all constructs before filling in the details. For example, the technique would recommend that you write "IF (condition) THEN" and "END IF;" and then fill in the middle. Similarly, you would write "convert_to_integer();" before filling in the value that you'd want to convert. In **Listing 1**, the comments tell the order in which I wrote the lines of code. The second technique Bill showed me was to indent my lines so the opening and closing constructs are on the same vertical column **(Listing 1)**. Then, indent all of the lines of code within that construct. Arranging them so makes the absence of the beginning or ending of the construct that much more visible.

Michael Bush, Codex's system administrator, also provided some insights into how he writes programs. Michael doesn't write programs sequentially. His technique is to write in sequence until he needs a procedure or a subprogram. Then, he writes the call inline and jumps to the declaration. Although he then writes the declaration statement, he doesn't fill in the details of the declaration until after he writes the main body of code. In this way, he ensures the consistency of the call and declaration by writing the statements at the same time.

During the project's planning stages, Bill and I had discussed having regular meetings at which we would evaluate our progress, look at and critique the models, and refine strategy. As we advanced into the project, those meetings became impractical. Both the model's complexity and Bill's schedule made detailed analysis time consuming and difficult to arrange. Although I hadn't been getting detailed comments on my modeling style since fairly early on in the design phase, when I finally decided to stop sending the model to Bill on a regular basis, I felt almost as a lion cub no longer under its mother's watchful eye.

Having written the first pass at a model, I needed to simulate and debug it. In the next article in the series, I will examine how I found and fixed the model's syntax and design errors. Simulating the design at the behavioral level using source-level debuggers may look different from the gate-level simulators you are used to, but they are far more similar than you might expect. EDN

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## References

1. *IEEE Standard VHDL Language Reference Manual*, IEEE Std 1076-1987, Institute of Electrical and Electronics Engineers Inc, New York, 1988.
2. *Z80 CPU Central Processing Unit Technical Manual*, Zilog Corp, September 1988.

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Article Interest Quotient
(Circle One)
High 506 Medium 507 Low 508

**Listing 1—VHDL architecture for reset state machine**

```
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Architecture Synthesizable of RESET is      -- 1st Declare the architecture
begin                                       -- 3rd Begin the architecture
   process                                  -- 4th Declare the process
      VARIABLE rst_act : Boolean := FALSE;  -- 6th Declare process variables
      VARIABLE clk_cnt_before : integer range 0 to 3 :=0;   -- 7th
               clk_cnt_after : integer range 0 to 3 :=0;    -- 8th
   begin                                    -- 9th Begin the process
      wait until clk'event and clk = '1';   -- 10th
      if ( RESET_n = '0' ) then             -- 11th Open the IF, THEN, ELSE
         rst_act := TRUE;                   -- 13th
         if ( clk_cnt_before = 3 ) then     -- 14th Open the embedded IF
               null;                        -- 16th
            else                            -- 17th
               clk_cnt_before := clk_cnt_before + 1;        -- 18th
         end if;                            -- 15th Close the embedded IF
      end if;                               -- 12th Close the IF, THEN, ELSE
   end process;                             -- 5th Close the process
end Synthesizable;                          -- 2nd Close the architecture
```

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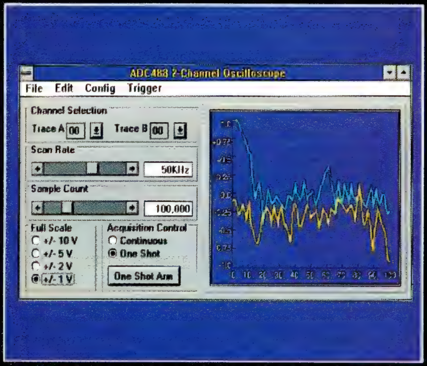

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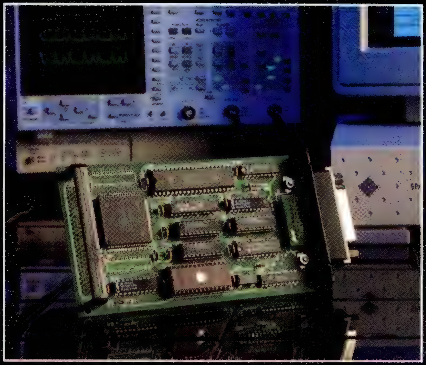

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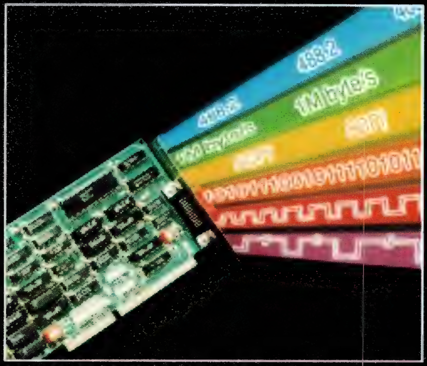

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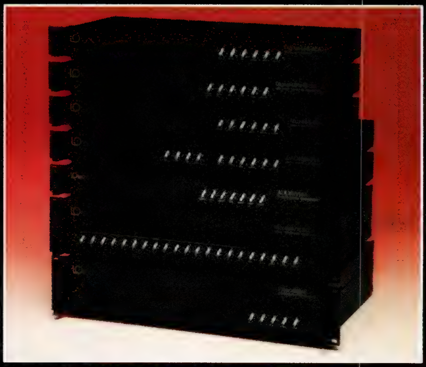

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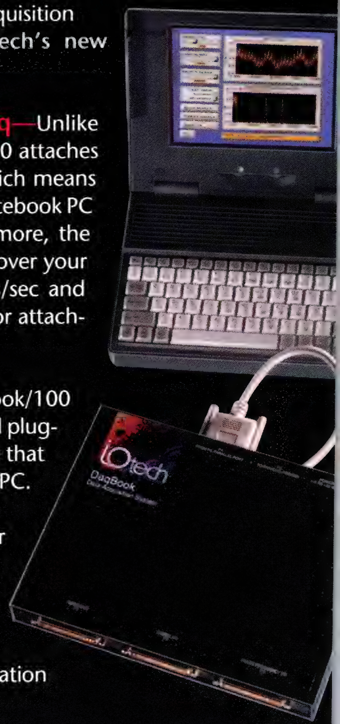

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# Getting the most out of redundant arrays of inexpensive disks

John McBride, Hewlett-Packard Co

***Large databases demand fault tolerance. Redundant arrays of inexpensive disks (RAIDs) can deliver, but first you've got to choose an architecture.***

In the 90s, as computer databases require more and more storage capacity, redundant arrays of inexpensive disks (RAIDs) are gaining in popularity. The six RAID architectures, or levels, let you have redundant data on an array of small hard-disk drives. (**Ref 1** describes five of the RAID architectures: RAID 1, 2, 3, 4, and 5.) Of the six, RAID 1 and RAID 5 are gaining the widest acceptance. To choose the right RAID architecture for your application, you must factor in such features as cost per megabyte, throughput per disk drive, and the hardware required to implement the array. Once you've chosen an architecture, you'll have to determine the best data-block size and how to minimize multiple drive accesses for single operations.

Both RAID 1 and RAID 5 describe block-striped arrays. Block striping divides data into multiple blocks, which an array controller stores in separate drives across the array and automatically balances the storage load across the array. The block size is the amount of contiguous data on a single disk. The advantage of block striping is that each drive can independently service a read request that is equal to or less than the block size.

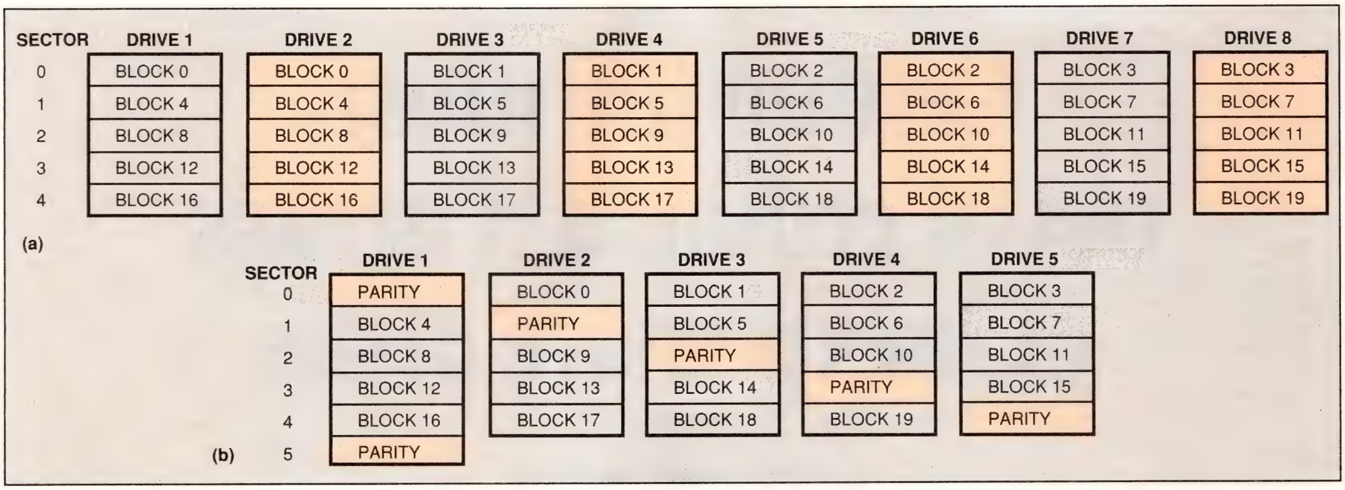
A RAID 1 array stores data with mirrored redundancy. Anytime the controller writes a block to a disk, it writes the same block to a mirror disk. A traditional mirrored pair of drives is the same as a 2-drive RAID 1 array.

A RAID 5 array block stripes data and a parity block for each array sector. If there are N drives in the array, the controller writes a different block of data to each of the N − 1 drives in the array. The controller writes a parity block for the data on the N − 1 blocks to the Nth drive in the array. As the controller continues to write more blocks to the array, the updated parity block rotates from one drive to the next drive (**Fig 1**). A 5-drive RAID 5 array with parity provides the same amount of storage as an 8-drive RAID 1 array with mirrored redundancy.

To take full advantage of a block-striped array, the array controller must be able to queue commands from the host. Command queuing lets the array service multiple I/O requests concurrently. When an array controller doesn't provide command queuing, the host computer can service only one transaction at a time. Without command queuing, the array behaves as a single disk drive with redundancy.

Block size is another important consideration. You should choose a block size large enough so that the majority of array accesses are within one block. Each access to the array that is larger than a block involves accessing two or more drives. Efficient command queuing can minimize the penalty paid for accessing more than one array for a single transaction. The trick is keeping all the drives busy through command reordering or data buffering. The penalty for too small a block size is less when all the drives are busy than when one drive is idle waiting for other drives to be free from a multiple-drive access.

To demonstrate the performance penalty you'll incur for an inadequate block size, consider an array with a block size smaller than the majority of accesses to the array. Let's say the host operating system requires 16-kbyte read operations from a RAID array with either 16- or 8-kbyte blocks. The first scenario has the host reading 16-kbyte blocks 20% of the time and 8-kbyte blocks 80% of the time. In the second scenario,



| SECTOR | DRIVE 1 | DRIVE 2 | DRIVE 3 | DRIVE 4 | DRIVE 5 | DRIVE 6 | DRIVE 7 | DRIVE 8 |
|---|---|---|---|---|---|---|---|---|
| 0 | BLOCK 0 | BLOCK 0 | BLOCK 1 | BLOCK 1 | BLOCK 2 | BLOCK 2 | BLOCK 3 | BLOCK 3 |
| 1 | BLOCK 4 | BLOCK 4 | BLOCK 5 | BLOCK 5 | BLOCK 6 | BLOCK 6 | BLOCK 7 | BLOCK 7 |
| 2 | BLOCK 8 | BLOCK 8 | BLOCK 9 | BLOCK 9 | BLOCK 10 | BLOCK 10 | BLOCK 11 | BLOCK 11 |
| 3 | BLOCK 12 | BLOCK 12 | BLOCK 13 | BLOCK 13 | BLOCK 14 | BLOCK 14 | BLOCK 15 | BLOCK 15 |
| 4 | BLOCK 16 | BLOCK 16 | BLOCK 17 | BLOCK 17 | BLOCK 18 | BLOCK 18 | BLOCK 19 | BLOCK 19 |

(a)

| SECTOR | DRIVE 1 | DRIVE 2 | DRIVE 3 | DRIVE 4 | DRIVE 5 |
|---|---|---|---|---|---|
| 0 | PARITY | BLOCK 0 | BLOCK 1 | BLOCK 2 | BLOCK 3 |
| 1 | BLOCK 4 | PARITY | BLOCK 5 | BLOCK 6 | BLOCK 7 |
| 2 | BLOCK 8 | BLOCK 9 | PARITY | BLOCK 10 | BLOCK 11 |
| 3 | BLOCK 12 | BLOCK 13 | BLOCK 14 | PARITY | BLOCK 15 |
| 4 | BLOCK 16 | BLOCK 17 | BLOCK 18 | BLOCK 19 | PARITY |
| 5 | PARITY | | | | |

(b)

**Fig 1—The RAID 1 and RAID 5 array architectures both offer redundant data storage for fault-tolerant applications. A RAID 1 array has a mirrored disk drive for every storage drive in the array (a). A RAID 5 array has a parity block for all the blocks of data contained in each array sector (b).**

the host reads 16-kbyte blocks 100% of the time. For an 8-kbyte block size, a 16-kbyte read operation requires access to two disk drives. (Note that write operations exhibit the same performance figures as reads.)

**Tables** 1 and 2 show typical performance figures for the two scenarios for the RAID 1 and RAID 5 architectures, respectively. The figures are based on the calculations performed in the **box,** "Insufficient block size degrades performance." Note that the degradation caused by a small (8-kbyte) block size is the same for both RAID arrays. You might expect that the number of I/Os per second would drop by 50% when a RAID 5 array performing 100% 16-kbyte reads changes from a 16-kbyte block size to an 8-kbyte block. However, these calculations were made assuming that all the disk drives are kept busy, so disk-drive accesses occur in parallel.

When a small portion (20%) of reads requires more data than an 8-kbyte block size, the performance penalty is small (14%). However, when all accesses exceed the block size, there is a severe penalty (43%) because two disk drives must service one request. Remember, these figures assume maximum concurrency. Degradation is considerably worse when the array controller doesn't access disk drives in parallel.

In the real world, not all—in fact, most—disk-drive accesses occur in parallel. One command-queuing technique to manage drive accesses efficiently is to have the array controller reorder requests. Reordering a request requires the host computer to keep track of which commands have been serviced and which have not. Reordering adds overhead to each command, which might negate its benefits. Another technique is to include a large data buffer (preferably greater than 1 Mbyte) to store data while the array controller waits for an available drive. To use a buffer, the host operating system must let commands execute out of order.

To illustrate the effects of inefficient disk-drive access consider a RAID 5 array comprising five drives and having a block size of 8 kbytes. Assume there are 100% 16-kbyte read operations and that the array controller doesn't reorder requests. If the first read operation accesses drives 2 and 3, then there are only two ways the second read can be concurrent with the first: The data must reside on drives 4 and 5 or drives 5 and 1. Because the RAID 5 architecture sequentially writes blocks of data to the drives on a rotating basis, the

## Table 1—Baseline RAID 1 performance

| Percentage of 16-kbyte reads | Block size | Baseline performance (I/Os/sec) | Degradation |
|---|---|---|---|
| 20% | 16 kbytes | 284 | 14% |
| 20% | 8 kbytes | 243 | |
| 100% | 16 kbytes | 254 | 43% |
| 100% | 8 kbytes | 146 | |

## Table 2—Baseline RAID 5 performance

| Percentage of 16-kbyte reads | Block size | Baseline performance (I/Os/sec) | Degradation |
|---|---|---|---|
| 20% | 16 kbytes | 178 | 14% |
| 20% | 8 kbytes | 152 | |
| 100% | 16 kbytes | 159 | 43% |
| 100% | 8 kbytes | 91 | |

## Insufficient block size degrades performance

Choosing the right block size is critical to an array's performance. Consider both an 8-drive RAID 1 array and a 5-drive RAID 5 array for two block sizes—8 kbytes and 16 kbytes. (An 8-drive RAID 1 array provides the same storage capacity as a 5-drive RAID 5 array.) In addition, assume that concurrency keeps all the disk drives busy. Now consider two scenarios: The first scenario is for 16-kbyte reads 20% of the time and 8-kbyte reads 80% of the time. The second is for 100% 16-kbyte reads.

Disk drives typically have:

- average seek time (with disk-controller overhead) = 15 msec
- single-spin rotational latency = 16.7 msec
- average rotational latency = (16.7 msec)/2 = 8.3msec
- data transfer rate = 2 Mbytes/sec.

First, we'll calculate the RAID 1 array performance for an 8-kbyte block size and 20% 16-kbyte reads and 80% 8-kbyte reads. The single-drive response time (SDRT) for 8-kbyte reads = average seek time + average rotational latency + time to transfer 8 kbytes from disk.

$$\text{SDRT} = 15 + 8.3 + (8192\ \text{bytes})/(2\ \text{Mbytes/sec}) = 27.429\ \text{msec.}$$

The single-drive transfer rate (SDTR) for reading an 8-kbyte block = 1/(SDRT) = 36.46 I/Os/sec.

For an 8-kbyte block size, a 16-kbyte read requires access to two drives, and an 8-kbyte read requires access to one drive. Therefore, there are six disk accesses for every five requests from the host under the first scenario. The transfer efficiency is then 5/6 × 100% = 83%.

The RAID 1 performance, or array transfer rate (ATR), for an 8-kbyte block size is 0.83 × number of drives × SDTR.

$$\text{ATR} = 0.83 \times 8 \times 36.46 = 243.05\ \text{I/Os/sec.}$$

Second, we'll calculate the RAID 1 array single-drive transfer rate (SDTR) for a 16-kbyte block size. Again, the scenario is 16-kbyte reads 20% of the time and 8-kbyte reads 80% of the time. The SDRT for a 16-kbyte block size = average seek time + average rotational latency + time to transfer 16 kbytes from disk.

$$\text{SDRT} = 15 + 8.3 + 16{,}384\ \text{bytes}/(2\ \text{Mbytes/sec}) = 31.525\ \text{msec.}$$

$$\text{SDTR} = 1/\text{SDRT} = 1/31.525 = 31.72\ \text{I/Os/sec.}$$

Because all read requests are equal to or less than the 16-kbyte block size, the number of read requests equals the number of disk accesses. Thus, the transfer efficiency is 100%. The RAID 1 array's transfer rate (ATR) = (fraction of 8-kbyte reads) × (number of drives) × (SDTR for 8-kbyte reads) + (fraction of 16-kbyte reads) × (number of drives) × (SDTR for 16-kbyte reads).

$$\text{ATR} = 0.8 \times 8 \times 36.46 + 0.2 \times 8 \times 31.72 = 284.08\ \text{I/Os/sec.}$$

Comparing the RAID 1 array performance for an 8-kbyte block size versus a 16-kbyte block size, the performance loss due to inadequate block size is

$$\text{loss} = ((284.08 - 243.05)/284.08) \times 100\% = 14.44\%.$$

### Change the drive number

The analysis for a RAID 5 architecture performing 80% 8-kbyte reads and 20% 16-kbyte reads is similar. The only difference is that there are five disk drives instead of eight. The RAID 5 performance loss due to inadequate block size turns out to be the same as for the RAID 1 array. Calculations for a 5-drive RAID 5 array yield

$$\text{ATR for 8-kbyte block size} = 151.91\ \text{I/Os/sec.}$$

$$\text{ATR for a 16-kbyte block size} = 177.55\ \text{I/Os/sec.}$$

$$\text{Performance loss} = ((177.55 - 151.91)/177.55) \times 100\% = 14.44\%.$$

To make the performance loss due to small block size more obvious, now consider the scenario for 100% 16-kbyte reads. An array with a 8-kbyte block size will always require two disk accesses for every 16-kbyte host request. Therefore, the array's transfer efficiency is 1/2 × 100% = 50%.

For 100% 16-kbyte reads, the performance of the RAID 1 array with an 8-kbyte block size is 50% × (number of drives) × (SDRT for an 8-kbyte block).

$$\text{ATR} = 0.5 \times 8 \times 36.46 = 145.83\ \text{I/Os/sec.}$$

For a 16-kbyte block size, the number of host accesses equals the number of disk accesses, so the transfer efficiency is 100%. For 100% 16-kbyte reads, the RAID 1 array's performance is (number of drives) × (SDRT for a 16-kbyte block size).

$$\text{ATR} = 8 \times 31.72 = 253.76\ \text{I/Os/sec.}$$

For 100% 16-kbyte reads, the RAID 1 array's performance loss due to inadequate block size is

$$\text{Loss} = (253.76 - 145.83)/253.76 \times 100\% = 42.53\%.$$

Similar analysis on the 5-drive RAID 5 array produces the same 42.53% performance loss.

total number of possibilities for a read operation is 5—drives 1 and 2, 2 and 3, 3 and 4, 4 and 5, and 5 and 1. Therefore, the probability that two read operations will be concurrent is $2 \div 5 = 0.4$.

To calculate the average concurrency for more than two read operations, you must analyze the joint probabilities for concurrency considering all possible read combinations. For the RAID 5 architecture, a Monte Carlo computer analysis determined the average concurrency for a number of requests ranging from 2 to 10 when there are 100% 16-kbyte reads and the block size is 8 kbytes (**Table 3**). The average concurrency asymptotically approaches 0.67 for a large number of requests. A similar analysis was performed for the RAID 1 architecture. The average concurrency asymptotically approaches 1.96 for a large number of requests (**Table 4**).

An array's performance is given by

$$\text{array I/O rate} = (1 + \text{average concurrency}) \times \text{single-drive I/O rate.}$$

The single-drive I/O rate is 36.46 I/Os per sec for the RAID 5 configuration and 31.72 I/Os per sec for the RAID 1 configuration. Column 3 of **Table 3** tabulates the RAID 5 array performance for M read requests. Column 4 tabulates the performance loss due to drive inactivity when read accesses aren't concurrent. The degradation is relative to the baseline RAID 5 performance tabulated in column 4 of **Table 2**. That performance assumed 100% 16-kbyte read operations, a 16-kbyte block size, and no idle drives.

Similarly, column 3 of **Table 4** tabulates the RAID 1 array's performance for M read requests. Column 4 shows the percentage degradation due to drive inactivity when read accesses aren't concurrent. The degradation is relative to the ideal RAID 1 performance tabulated in column 4 of **Table 1,** where 100% 16-kbyte read operations access a 16-kbyte block size and all drives are busy. The results of **Tables 3** and **4** display a marked performance degradation from the situation where all disk drives are busy. Computing the average concurrency is quite complex when you have a mixture of 16- and 8-kbyte reads. But the bottom line is that an array's performance is severely limited when disk drives remain idle while waiting for another drive.

## Table 3—Average concurrency for RAID 5 array

| Number of reads | Average concurrency | Array performance (I/Os/sec) | Performance loss due to drive inactivity relative to baseline performance |
|---|---|---|---|
| 2 | 0.4 | 51 | (159-51)/159 = 0.68 |
| 3 | 0.56 | 57 | (159-57)/159 = 0.64 |
| 4 | 0.62 | 59 | (159-59)/159 = 0.63 |
| 10 | 0.67 | 61 | (159-61)/159 = 0.62 |

## Table 4—Average concurrency for RAID 1 array

| Number of reads | Average concurrency | Array performance (I/Os/sec) | Performance loss due to drive inactivity relative to baseline performance |
|---|---|---|---|
| 2 | 1.0 | 73 | (254-73)/254 = 0.71 |
| 3 | 1.56 | 94 | (254-94)/254 = 0.63 |
| 4 | 1.81 | 103 | (254-103)/254 = 0.60 |
| 5 | 1.91 | 106 | (254-106)/254 = 0.58 |
| 10 | 1.96 | 108 | (254-108)/254 = 0.57 |

When the block size is chosen so that most of the accesses are smaller than the block size, there's still the possibility that the controller will have to access disks having data that aren't aligned with the block boundaries. Misalignment means that the controller must access data that straddles the boundaries of two blocks. If the block size is 8 kbytes and all 8-kbyte accesses are aligned with the block boundaries, then all 8-kbyte accesses require only one disk to service the request. If the data and boundaries aren't aligned, some requests may require access to two drives.

For example, if a host computer typically reads data from a 512-byte logical sector for a single disk drive, every 8-kbyte data transfer will require reads from 16 array sectors. If the host randomly chooses any sector as a starting sector, then 93.75% (15/16) of the starting addresses won't be aligned with the array's 8-kbyte block boundary.

Misalignment results in the same problem as having the wrong block size: Two drives must accommodate a single request. Even worse, misalignment requires two drive seeks to service an 8-kbyte request whereas an 8-kbyte block size requires two seeks for 16 kbytes—twice the data. The throughput penalty in megabytes per second will be less for misalignment than for a too-small block size. If possible, the file system could correct for misalignment by reordering the requests to ensure that all array accesses are aligned with the block boundaries. You can also correct for alignment errors by using a larger block size, such as 32 kbytes. However, large block sizes can negate the benefit of automatic load balancing across the array.

Finally, you should look at the pros and cons of RAID 1 and RAID 5 to determine which architecture is most appropriate for your application. The primary reason for RAID 5's recent popularity is that the architecture requires fewer redundant disk drives and therefore has a lower cost per megabyte than RAID 1. However, RAID 1 arrays have a higher throughput

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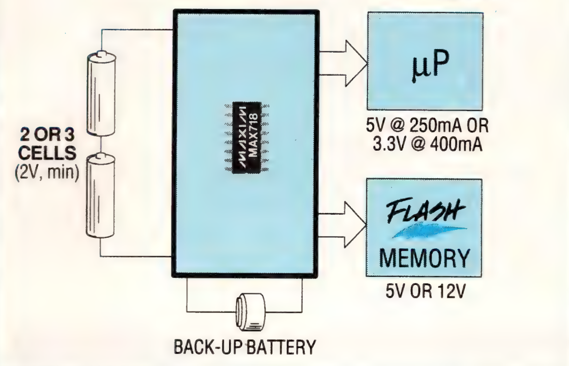
These dual-output switching regulators provide an unbeatable combination of high efficiency, low supply current, and small size. They fit perfectly in palmtop and other battery-powered microprocessor system designs. Integrated features include low-output-voltage warning, automatic switch-over between battery power and wall-adaptor power, logic output signalling when wall-adaptor is in use, and a mini back-up switcher powered by the back-up battery to keep-alive memory and clock.

- **Main Output: 3V or 3.3V or 5V**
- **Flash Programming Output: 5V or 12V**
- **87% Efficiency**
- **60µA Quiescent Current (20µA in Shutdown)**
- **Back-Up Battery Switchover**
- **Logic-Controlled Outputs**
- **Narrow 16-Pin SOIC**
- **$5.95***

**DUAL-OUTPUT REGULATOR POWERS µP & PROGRAMS FLASH**



| Part | Main Output | Wall-Adapter Detect Signal | Back-Up Keep-Alive Switcher | Total Shutdown |
|---|---|---|---|---|
| **MAX717** | 3.3V | YES | YES | NO |
| **MAX718** | 3.3V or 5V | NO | YES | NO |
| **MAX719** | 3.0V or 5V | NO | YES | NO |
| **MAX720** | 3.3V or 5V | YES | NO | YES |
| **MAX721** | 3.0V or 5V | YES | NO | YES |

* 1000-up, US recommended resale.

## Order a Pre-Built Evaluation Kit

The complete surface-mount MAX718 evaluation kit saves hours of component gathering and board design, layout, and assembly time. Order the MAX718EVKIT-SO, $30.00.

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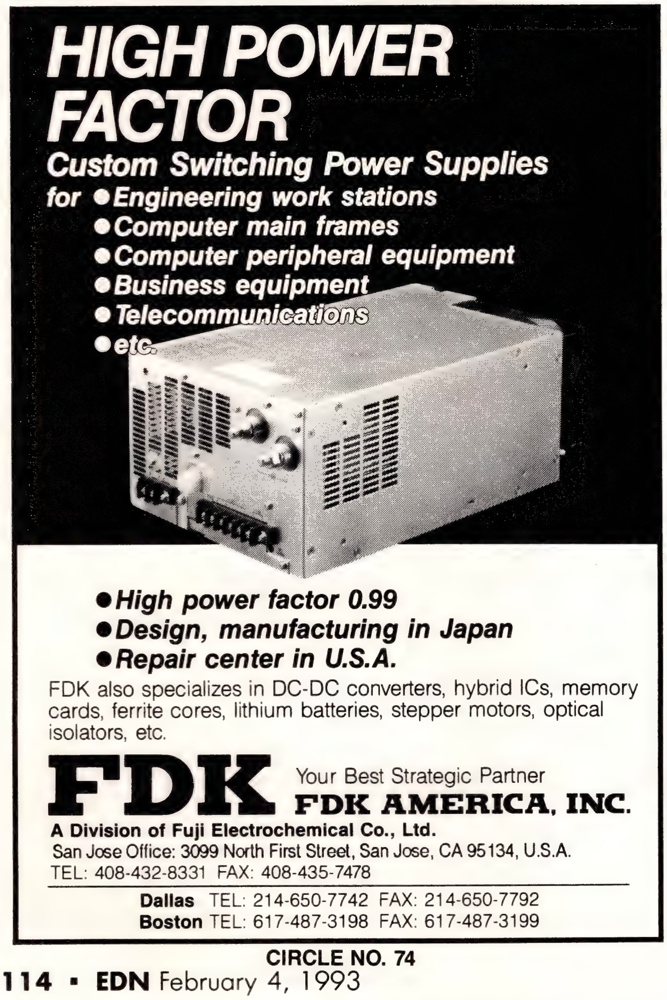

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CIRCLE NO. 74

per disk drive when there is a small number of transactions (see the analysis in **Ref 2**). Also, RAID 1 is simpler to implement. RAID 5 requires extra hardware buffers and firmware to handle read-modify-write cycles for updating the parity block.

RAID 5 write operations are much more complicated than those for RAID 1. In order to keep the parity block current, the controller requires four accesses to write data to a RAID 5 array: read data, read parity, write data, and write parity. In contrast, a controller only has to write to both drives in a mirrored pair when writing to a RAID 1 array. Also, a write to a RAID 1 array can be broadcast to all drives in the array. RAID 5 writes cannot be broadcast to other array drives.

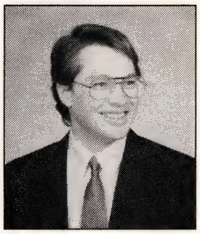
The overriding performance limiter in disk arrays is having multiple disk accesses servicing a single request from the host. Because RAID 5 requires more accesses to perform a write, the drives can be idle while waiting to complete the write operation. RAID 5 is not the best choice in applications requiring a small amount of transactions. However, for large databases that must handle many transactions, the lower cost of a RAID 5 array certainly justifies its use. EDN

## References

1. "A Case for Redundant Arrays of Inexpensive Disks (RAIDs)," D Patterson, D Gibson, and R Katz, ACM SIGMOD conference proceedings, Chicago, IL, June 1 to 3, 1988, pp 109 to 116.

2. *An evaluation of Redundant Arrays of Disks using an Amdahl 5890*, P Chen, MS Report, University of California at Berkeley, Dept of Electrical Engineering and Computer Science, Computer Science Div.

## Author's biography



*John G McBride has worked as a development engineer for Hewlett-Packard for the past five years. He currently works at the Boise Printer Div in Boise, ID, where he models and designs PC network servers and does PC test development. He was instrumental in the design of the HPC2425 SCSI disk array and HPC2201/C2204 fiber-link disk drives. John has a BSEE from Brigham Young University (Provo, UT) and an MSEE from Stanford University (Stanford, CA). His hobbies include white water rafting and being an assistant scoutmaster of a local boy scout troop. John is married and has two children.*

Article Interest Quotient (Circle One)
High 503 Medium 504 Low 505

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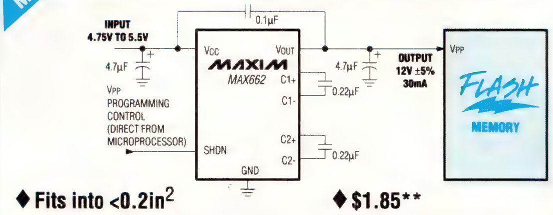

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**MAX734**

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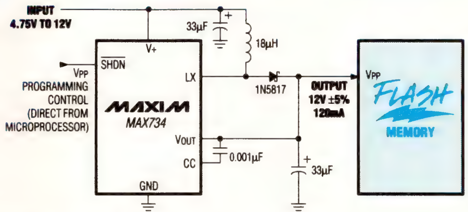

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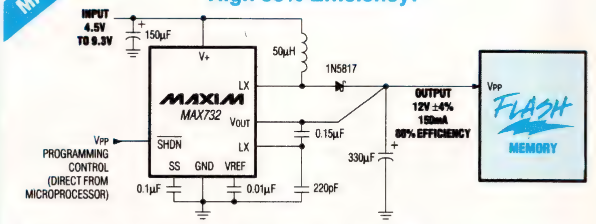

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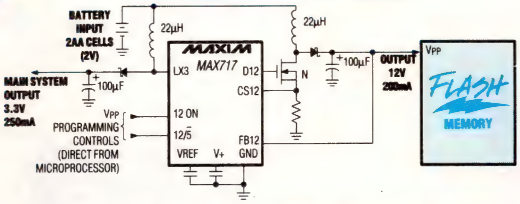
BATTERY INPUT 2AA CELLS (2V)
22µH
22µH
MAXIM
MAX717
LX3
D12
CS12
12 ON
12/5
FB12
VREF
V+
GND
N
MAIN SYSTEM OUTPUT 3.3V 250mA
100µF
100µF
VPP PROGRAMMING CONTROLS (DIRECT FROM MICROPROCESSOR)
OUTPUT 12V 200mA
VPP
FLASH MEMORY

- ◆ Flash Programming Supply and Main System Supply in Single IC
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†To order samples please call 1-800-998-8800. *Evaluation Kits available after November, 1992. Price does not include postage and handling.
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# LOWEST NOISE OP AMPS FOR ±5V SYSTEMS

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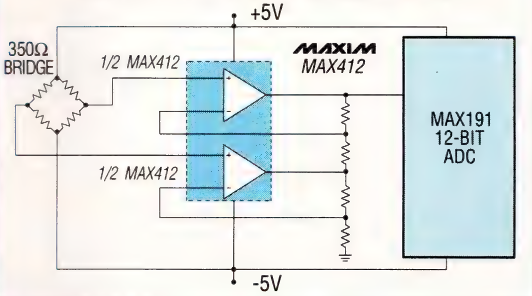
- ◆ **±2.4V to ±5V Supply Range**
- ◆ **28MHz Unity-Gain Bandwidth**
- ◆ **2.5mA Supply Current**
- ◆ **MAX412 Dual in 8-pin SO**
- ◆ **MAX414 Quad in 14-pin SO**

### Eliminate ±15V Amplifiers



## Choose the Lowest Noise, Precision Op Amp Solutions

| | Op Amps Per Pkg | Noise (nV/√Hz Max) | $V_{OS}$ (μV Max) | Bandwidth (MHz) | $A_{VOL}$ (dB Min) | Supply Range | Price† ($) |
|---|---|---|---|---|---|---|---|
| **MAX410** | 1 | 2.4 | 250 | 28 | 115 | ±2.4V to ±5V | 1.50 |
| **MAX412** | 2 | 2.4 | 250 | 28 | 115 | ±2.4V to ±5V | 2.45 |
| **MAX414** | 4 | 2.4 | 320 | 28 | 115 | ±2.4V to ±5V | 4.50 |
| **MAX427** | 1 | 3.8 | 15 | 6 | 137 | ±15V | 1.83 |
| **MAX437** | 1 | 3.8 | 15 | 60<br>(Av ≥ 5V/V) | 137 | ±15V | 1.83 |

† 1000 up, Suggested Resale FOB USA, MAX410/12/14 B-grade Pricing.

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1μA Op Amp Extends Battery Life 15X

Output Swings Rail-to-Rail, Drives 2000 Times Supply Current

Before the MAX406, 15μA supply current was considered a state-of-the-art micropower op amp. The MAX406 has now redefined the term micropower by operating at only 1μA. If batteries had an indefinite shelf-life, the MAX406 could operate up to 250,000 hours (28 years) from a 250mA-hr lithium coin cell. Drawing no more than battery leakage current, battery-powered systems can operate over 15 times longer. The MAX406 operates from a single 2.5V to 10V supply, or dual supply from ±1.25 to ±5V.

The MAX406 is unity gain stable. For high-speed applications, pin 8 can be connected to the positive supply for a 20V/μs slew rate and a 40kHz gain bandwidth (AVCL ≥ 2V/V), without drawing any extra supply current. The MAX406 also offers superior stability compared to other micropower CMOS op amps—it remains stable while driving capacitive loads as high as 1μF without oscillating.

Lowest Noise & Drift, Highest Gain Op Amps

New Edition!

The MAX426 is stable for gains ≥ 30V/V and offers a 15MHz gain-bandwidth product, 12V/μs slew rate, and DC performance equivalent to the MAX425. Applications include weigh-scales, sensors, low frequency active filters, current-to-voltage converters, and S/H amplifiers.

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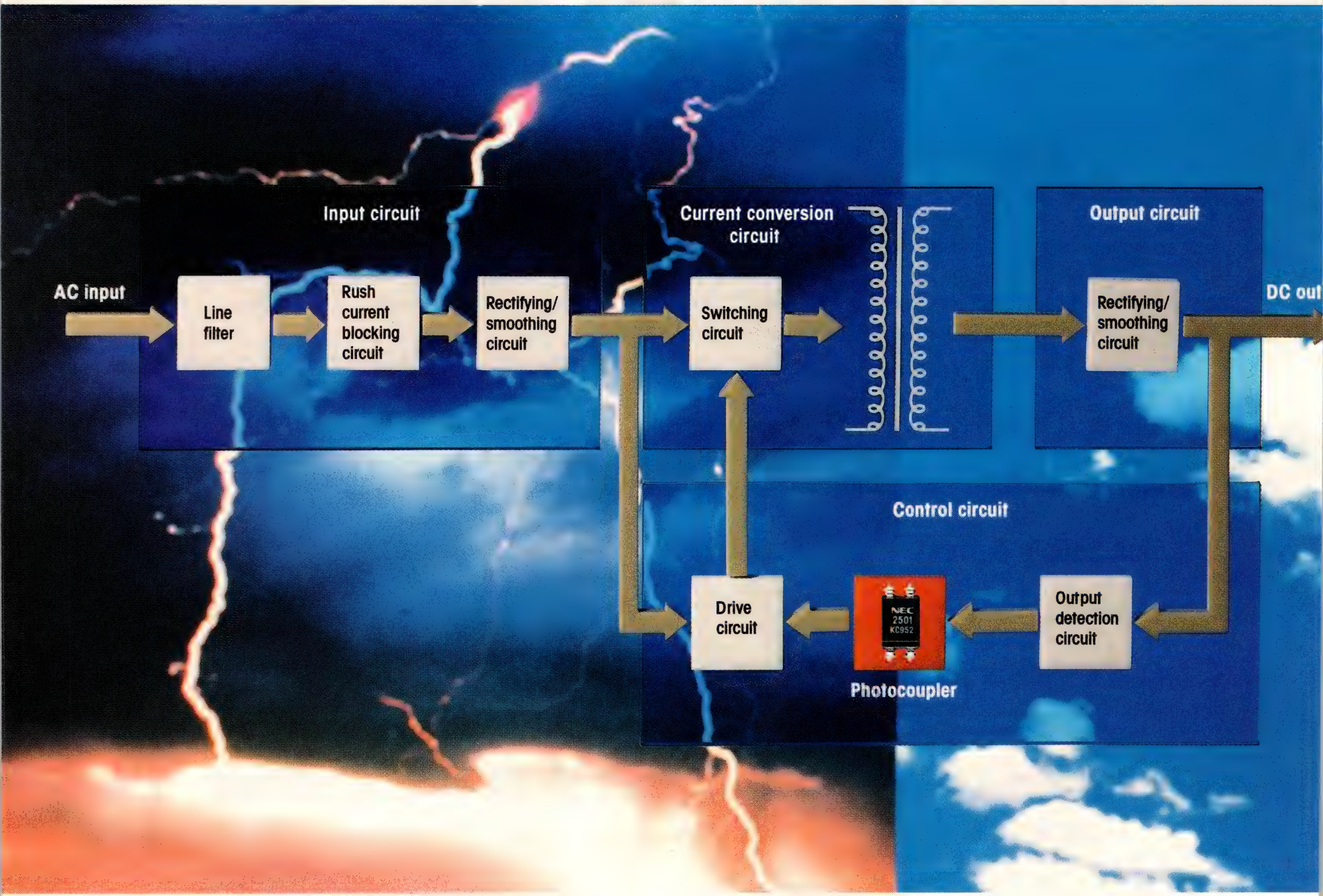
# Phenomenal Photocouplers.



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NEC photocouplers give you exceptional isolation and resistance to heat and humidity.

☐ 5.0kV r.m.s./minute.

☐ PCT>200 hours.

They satisfy your needs for UL1557, BS415 and VDE0884 safety standards.

Our photocouplers come in a wide variety of types in 4-pin or 6-pin DIP, including DC- or AC-input and single- or darlington-transistor output. They are designed for problem-free reflow soldering.

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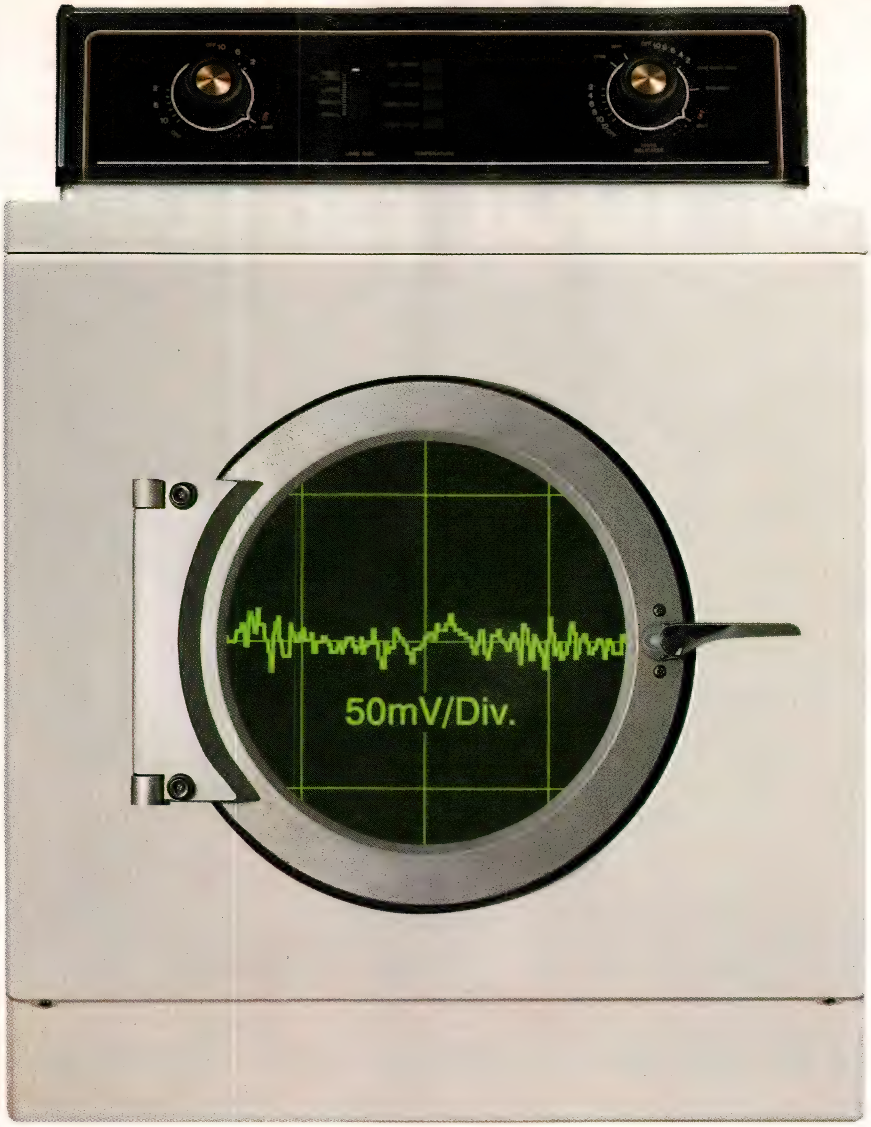
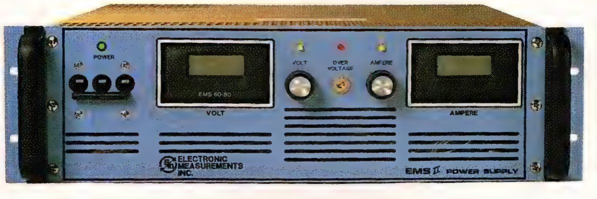


# EMS II High Power Switchers. You've never seen power this clean.

The new EMS II Series Switch Mode DC Power Supplies give you clean power, every time...with no glitches, spikes or headaches. In fact, they handle the highest load of power per cubic inch in the industry. Here are some more features to make your decision easier:



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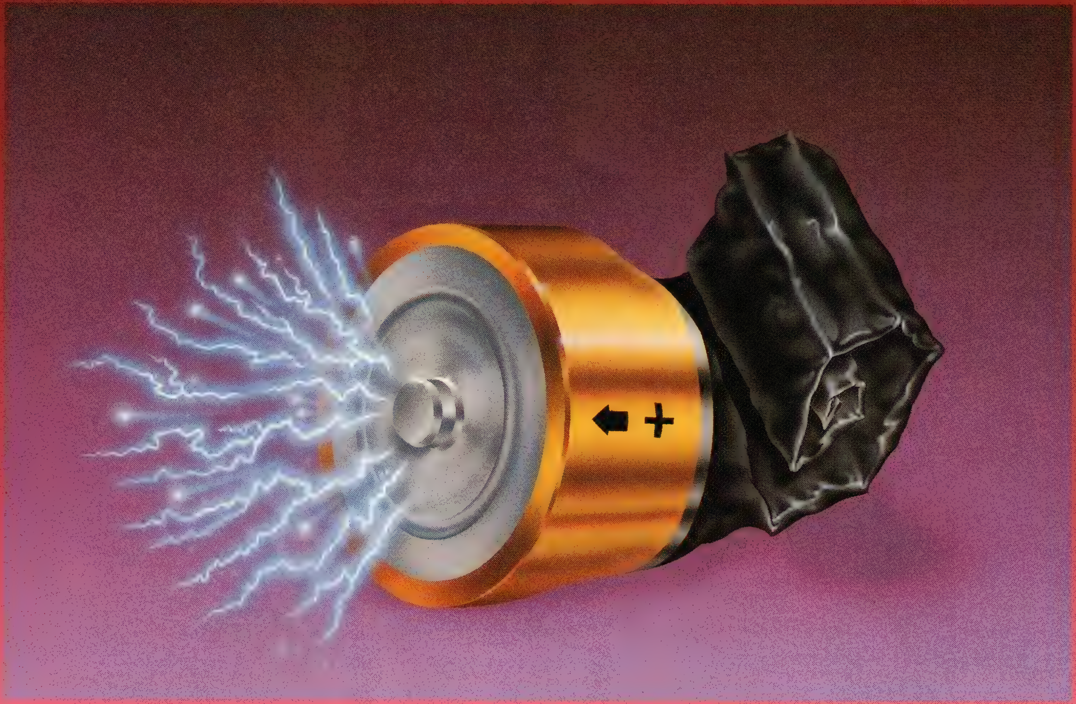
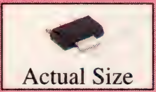
CIRCLE NO. 79

# Squeeze More Life Out of Your Battery...



## With the LT1121 Micropower Low Dropout Regulator.



Squeeze more life out of your battery with the LT1121 micropower low dropout regulator from Linear Technology. The LT1121 features a dropout voltage of 0.4V and quiescent current of just 30µA, yet supplies up to 150mA of output current. The 8 pin versions include a shutdown pin dropping quiescent current to a mere 15µA. Unlike many older devices, ground current does not increase significantly when the device operates in dropout.

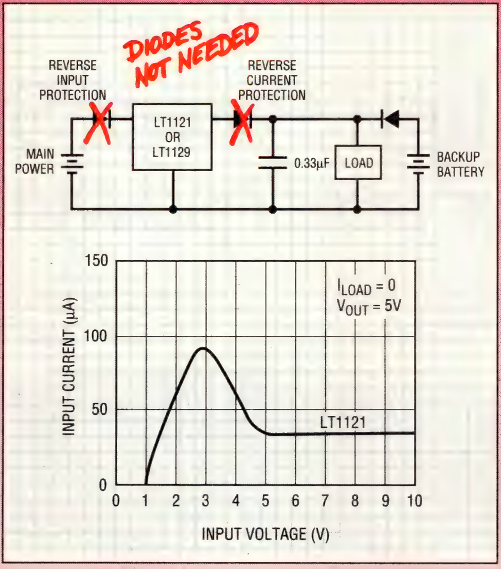
The LT1121 saves board space since it can operate with small surface mount ceramic 0.33µF capacitors at the output versus older devices which require 1µF to 100µF for stability.

The LT1121 is ideal for battery powered and battery back-up circuits. The LT1121 has built-in protection against reverse input voltages up to 30V below ground and output shorts to negative voltages, eliminating the need for protection diodes.

If the output is held high by a back-up battery while the input pin is pulled to ground or reversed, the LT1121 will not discharge the battery. No reverse current will flow from the output back to the input and only 16µA will flow from the output pin to ground.

The LT1121 is supplied in 8-lead SOIC, DIP, SOT-223 and TO-92 packages. The LT1121 is available with fixed output voltages of 3.3V and 5V and an adjustable version with an output voltage range of 3.8V to 20V. For higher output currents, up to 700mA, the LT1129 can be used. The LT1129 has all the features of the LT1121 with only a small increase in quiescent current to 60µA.

Pricing in 1000 up quantities for the LT1121 in SOT-223 is $1.67. For details, contact Linear Technology Corporation, 1630 McCarthy Blvd., Milpitas, CA 95035 / 408-432-1900. For literature only call **800-637-5545.**



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CIRCLE NO. 80

# Simulation technique emulates oscilloscope

**Alan Wolke, AMP Inc, Somerville, NJ**

Using the following technique, you can make your simulator act like an oscilloscope by displaying repetitive waveforms vs an arbitrary fixed-frequency reference. The simulator display is similar to the display on an oscilloscope triggered from the same reference. One example in which this technique is useful is analyzing transition time deviations, or jitter, of a digital communications signal.

The trick is to emulate the horizontal sawtooth oscillator in the oscilloscope and display your waveform vs the sawtooth, just like the old recurrent sweep scopes do. Using the Probe function available in a commercial version of Spice (PSpice of Microsim Corp, Irvine, CA), you can generate the sawtooth wave using the following statement:

$$\mathrm{scope}(t,d) = t * \left[ \frac{\mathrm{a\,tan}\left(\tan\left(\dfrac{\pi * (\mathrm{time} - d - \frac{t}{2})}{t}\right)\right)}{\pi} + \frac{1}{2} \right] \qquad (1)$$

In the equation, *time* is the sweep variable time from the transient analysis; t is the sawtooth period, which is also the desired time window; and d is the sawtooth delay, or retrace location in time.

If your simulator or postprocessor supports the MOD function, the sawtooth-generator statement is as simple as (time − d)MOD(t). The simulator used in this example lets you define functions in a macro file called PROBE.MAC. The following two lines in a PROBE.MAC file use the SCOPE(t,d) sawtooth function:

$$\mathrm{pi} = 4 * \mathrm{a\,tan}(1)$$

$$\mathrm{scope}(t,d) = t * (\mathrm{a\,tan}(\tan(\mathrm{pi} * (\mathrm{time} - d - t/2)/t))/\mathrm{pi} + 1/2) \qquad (2)$$

**Fig 1a** shows the simulated output of a simple differential amplifier vs time. The input to the amplifier is a 50% duty-cycle bit stream. Analyzing the deviation of each transition time from its ideal position would involve tedious zooming and recording of data at each edge.

However, **Fig 1b** shows the same waveform plotted over a repetitive 24-nsec window. You produce this waveform by changing the $x$-axis variable in **Eq 1** from the sweep variable *time* to the function scope(t,d) in **Eq 2.** In other words, you change the $x$ axis from a linear time variable to a sawtooth variable.

For example, changing the $x$-axis variable to SCOPE(24n,0) creates a sawtooth that starts at 0 nsec when time = 0, ramps up to 24 nsec, and then repeats. This creates an overlay of 0- to 24-nsec segments. You can use the variable d, which is set to 0 in this case, to slide the waveform window in time. Proper selection of t and d will result in a synchronized recurrent sweep that determines whether the simulator's retrace signal is buried under the signal (as it is in this example) or readily discernible. **EDN BBS /DI_SIG #1207**

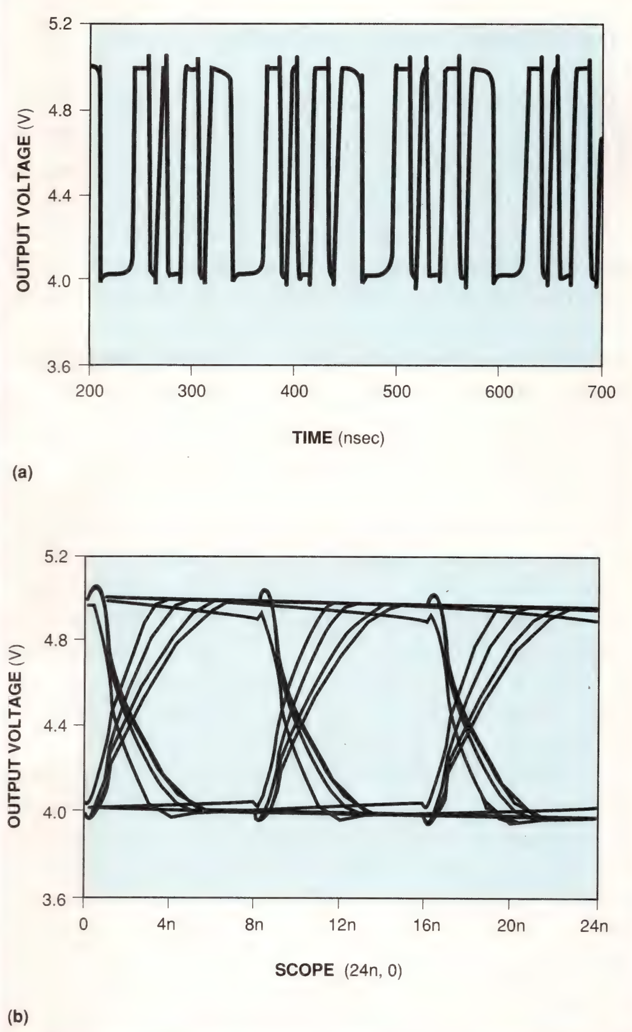


**Fig 1—The standard simulator output of voltage vs time (a) doesn't let you easily analyze transition deviations of a repetitive waveform. However, changing the *x*-axis variable from time to a sawtooth waveform produces overlapping waveforms, or eye patterns (b). This display lets you analyze transition deviations more easily.**

**To Vote For This Design, Circle No. 391**

# Laser-diode model accounts for temperature

**Lawrence G Meares, Intusoft, San Pedro, CA**

Simulating the output power of a laser as temperature changes is an important but difficult task. An increase in optical output power accompanied by a decrease in temperature can cause laser burnout. This laser-diode model includes a second diode that monitors changes in optical power with temperature. You can use the output of the monitor diode to change the bias of the laser diode.

**Fig 1** shows the laser-diode subcircuit; **Listing 1** is the corresponding netlist. The areas within dashed lines indicate external components used for testing only. D1 (DLASER) provides the voltage and current characteristics of the laser and will exhibit variations in operating point vs temperature. In this particular case, D1 is a macromodel of the Hitachi HL7801E GaAlAs laser diode. To adapt the model to other laser diodes, adjust the energy gap (EG), saturation-temperature exponent (XTI), and saturation current (IS) to provide the correct voltage and current response vs temperature. You can use the .TEMP command to alter the laser's operating temperature.

The remainder of the subcircuit model generates the proper monitor-diode current. The standard Spice diode produces an increase in current flow with temperature. To generate a negative-temperature-coefficient response to optical power, the model uses the arrangement of H1, R3, I2, and D2. Along with D2, H1's multiplying constant, R3's temperature coefficient, and I2's current establish the monitor-diode-current vs forward-current response. The laser-diode response is much faster when the diode is turned on than when it is turned off. C1 and R1 control the impedances of the model and thus the response performance. When the diode is in the low power region, the time constant set by R1 and C1 sets the response time at 5 nsec. At higher power levels, the RC impedance becomes negligible, and the response time of the diode decreases.

This model sets the capacitance of D3 at 5 pF to mimic the transient performance of the actual monitor diode. G1 uses a conversion factor of 0.0012 to convert its input, which is analogous to the optical power, into the proper scaling units for the monitor-diode current. This configuration lets you use the monitor diode to control the biasing of the laser diode. **EDN BBS / DI_SIG #1208**

**To Vote For This Design, Circle No. 392**

### Listing 1—Spice netlist for laser diode

```
.SUBCKT LASER  2  3  11  10
*Laser Diode   A  C  |   |
*Monitor Diode        A   C
D1 1 3 DLASER
.MODEL DLASER D(RS=1.5 EG=2.8 XTI=3 N=1 IS=1E-30)
H1 7 0 V1 24
D2 8 9 DIODE3
.MODEL DIODE3 D(EG=0)
R1 9 0 100
G1 10 11 9 0 .0012
D3   11   10   DIODE
.MODEL DIODE D(CJO=5PF)
R3 7 8 1 TC=.0085
I2 8 7 .9
C1 9 0 50P
V1 2 1
.ENDS
```

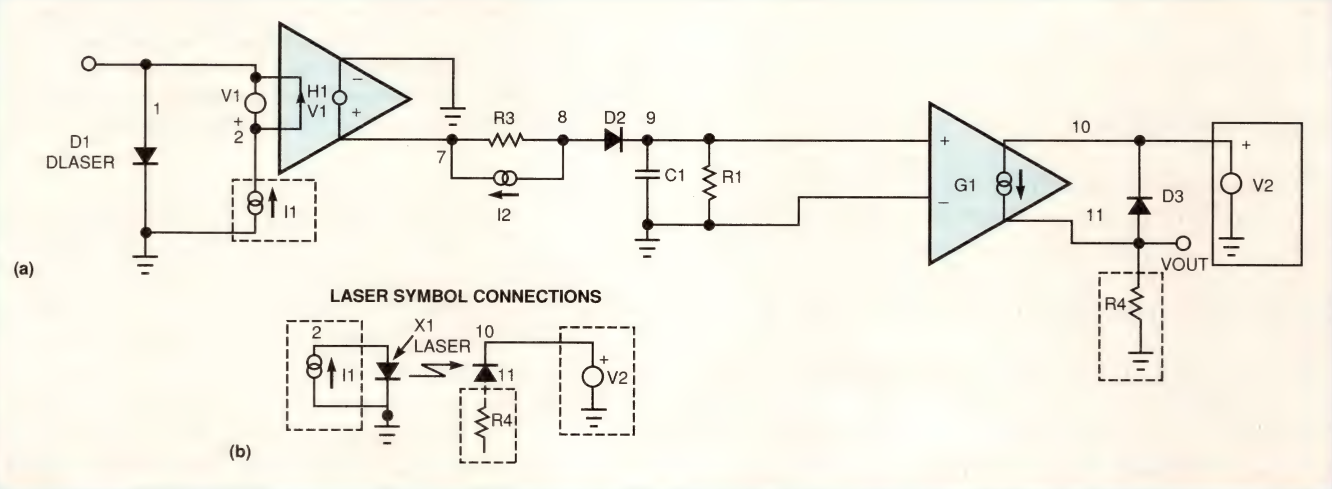
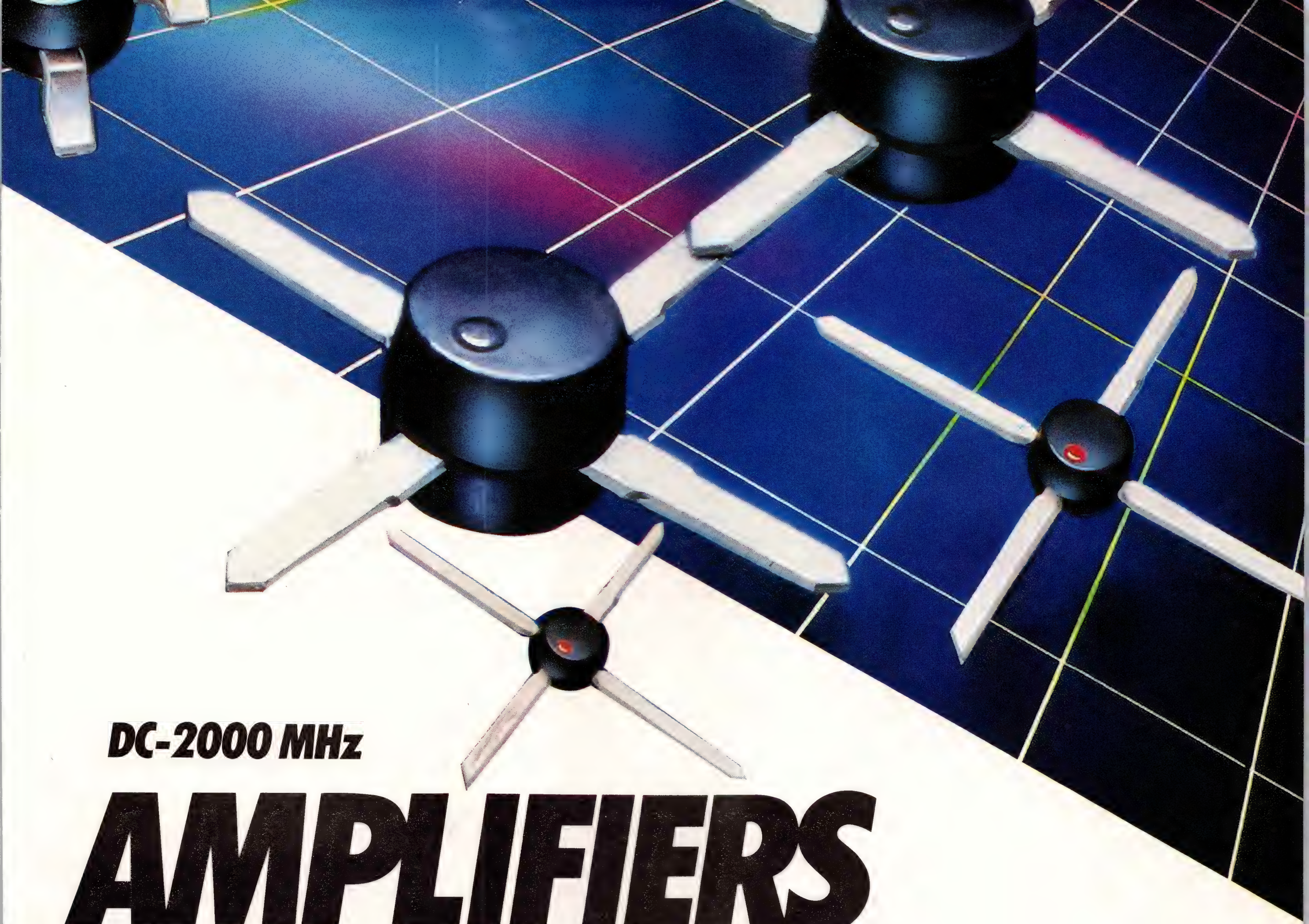


**Fig 1—The expanded laser-diode model (a) shows a monitor diode, which keeps track of the change in output power with temperature. How the model would appear on a schematic is shown in (b).**



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| | MAV-1<br>1.15 | +MAV-2<br>1.45 | +MAV-3<br>1.55 | MAV-4<br>1.65 | | | | MAV-11<br>2.15 |
| CERAMIC SURFACE-MOUNT | RAM-1<br>4.95 | RAM-2<br>4.95 | RAM-3<br>4.95 | RAM-4<br>4.95 | RAM-6<br>4.95 | RAM-7<br>4.95 | RAM-8<br>4.95 | |
| PLASTIC FLAT-PACK | MAV-1<br>1.10 | +MAV-2<br>1.40 | +MAV-3<br>1.50 | +MAV-4<br>1.60 | | | | MAV-11<br>2.10 |
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| Freq.MHz,DC to | 1000 | 2000 | 2000 | 1000 | 2000 | 2000 | 1000 | 1000 |
| Gain, dB at 100MHz | 18.5 | 12.5 | 12.5 | 8.3 | 20 | 13.5 | 32.5 | 12.7 |
| Output Pwr. +dBm | 1.5 | 4.5 | 10.0 | 12.5 | 2.0 | 5.5 | 12.5 | 17.5 |
| NF, dB | 5.5 | 6.5 | 6.0 | 6.5 | 3.0 | 5.0 | 3.3 | 3.6 |

Notes: + Frequency range DC-1500MHz ++ Gain 1/2 dB less than shown

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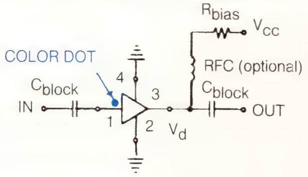
| 120 x 60 | .022, .047, .068, .1$\mu$f |

Typical Circuit Arrangement



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CIRCLE NO. 81

# Behavioral model emulates universal filter

**Bashir Al-Hashimi, Matthey Electronics, Stoke-on-Trent, UK**

**Listing 1** is a behavioral model implemented in PSpice (Microsim Corp (Irvine, CA)) that simulates lowpass, highpass, and bandpass filters using the Laplace function. The model can simulate second-order and unity-gain filters of various types including Butterworth, Chebyshev, and Bessel. The behavioral model treats a circuit like a black box, which you can describe using an equation or table.

The model cascades a highpass and lowpass filter. The transfer functions of the highpass and lowpass filters, respectively, are as follows:

$$\frac{V_{OUT}}{V_{IN}} = \frac{S^2}{S^2 + d2S + a1}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{a3}{S^2 + a4S + a3}$$

where a1, a2, a3, and a4 are expressions describing the filter characteristics. The model expresses these equations using Laplace descriptions of voltage-controlled voltage sources. Nodes 1 and 2 are the input and output of the highpass filter, and nodes 2 and 3 are the input and output of the lowpass filter, respectively.

## Table 1—Filter-function settings

| Filter | FC1 | FC2 |
|---|---|---|
| Lowpass | Small | Required 3-dB point |
| Highpass | Required 3-dB point | Large |
| Bandpass | Lower 3-dB point | Upper 3-dB point |

## Table 2—Filter-parameter settings

| Filter type | Omega | Q |
|---|---|---|
| Butterworth | 1 | 0.707 |
| Chebyshev (0.5 dB) | 1.231 | 0.864 |
| (1 dB) | 1.05 | 0.957 |
| (2 dB) | 0.907 | 1.129 |
| (3 dB) | 0.841 | 1.307 |
| Bessel | 1.73 | 0.577 |

To use the model to simulate a particular filter function, you specify the parameter values of FC1 and FC2, which are the 3-dB frequency points of the highpass and lowpass filters, respectively. To simulate an overall highpass-filter response, FC2 needs to be sufficiently large so it won't interfere with the action of the highpass filter. **Table 1** presents the available options. You can use **Table 2** to choose the omega and Q parameters to achieve the particular filter characteristics. Note that this simulation method is independent of the actual filter's technology and is equally applicable to passive, active, switched, and digital filters. **EDN BBS /DI_SIG #1209**

**To Vote For This Design, Circle No. 393**

## Listing 1—Universal-filter netlist

```
.PARAM omega={-}                        ;  see table.2
.PARAM Q={-}                            ;  see table.2
.PARAM Fc1={-}                          ;  Highpass 3dB frequency point
.PARAM Fc2={-}                          ;  Lowpass 3dB frequency point
.PARAM PI={3.1416}                      ;  Constant
.PARAM PI_SQUARE={PI*PI}                ;  Constant
.PARAM a1={omega*omega*4*PI_SQUARE*Fc1*Fc1}  ; Highpass filter parameters
.PARAM a2={2*PI*Fc1*omega/Q}                 ;
.PARAM a3={omega*omega*4*PI_SQUARE*Fc2*Fc2}  ; Lowpass filter parameters
.PARAM a4={2*PI*Fc2*omega/Q}                 ;
*Filter model description*
EHIGH 2 0 LAPLACE {V(1)}={(S*S)/(S*S+a2*S+a1)} ; Eq.(1) Pspice text code
ELOW  3 0 LAPLACE {V(2)}={(a3)/(S*S+a4*S+a3)}  ; Eq.(2) Pspice text code
```

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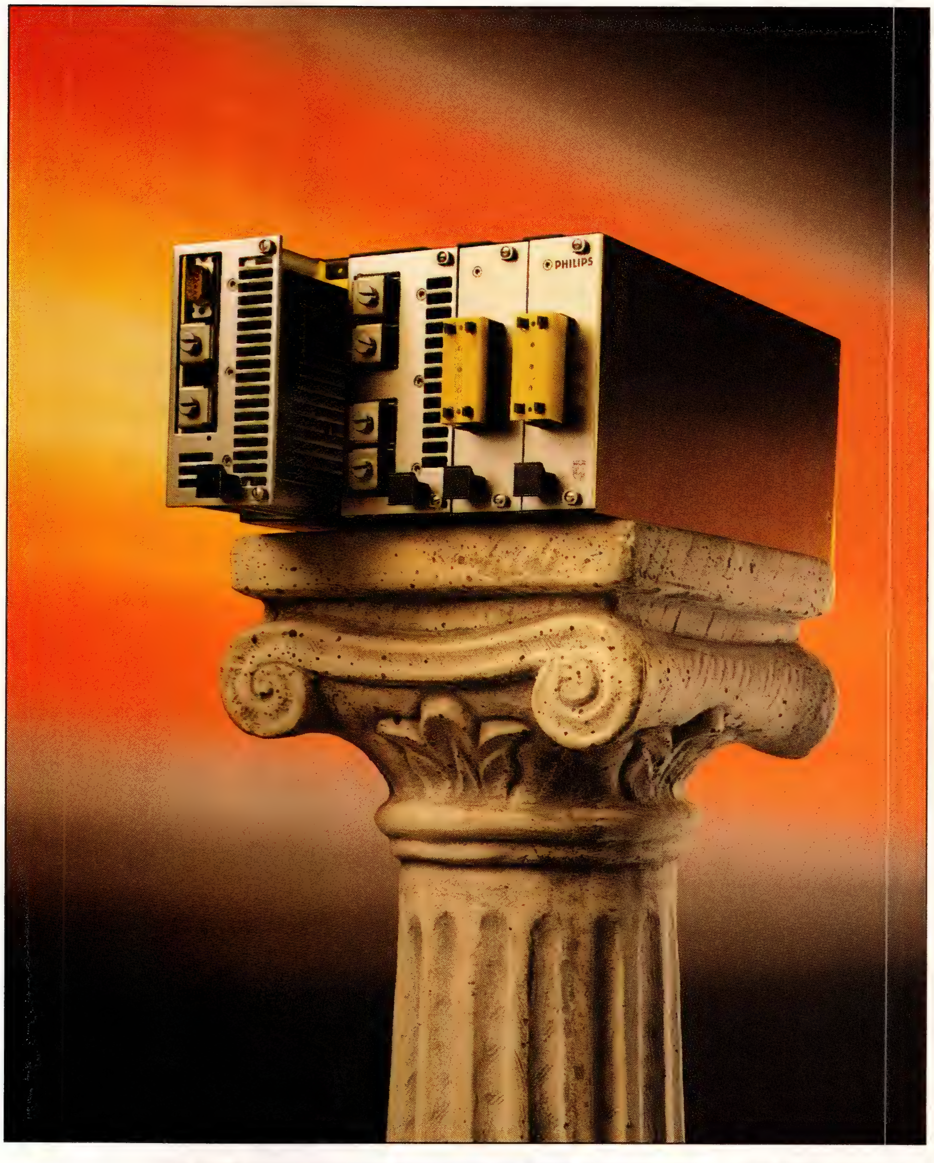

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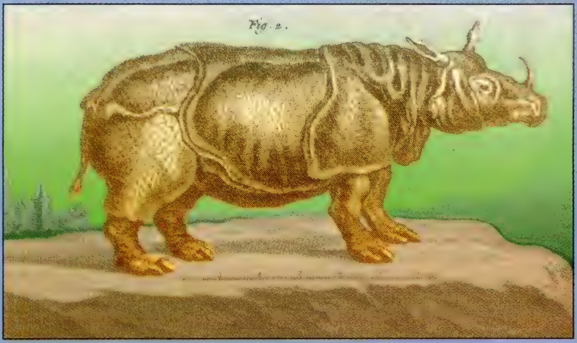

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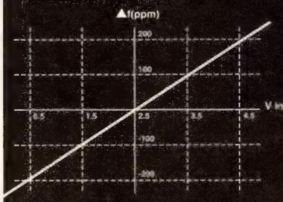

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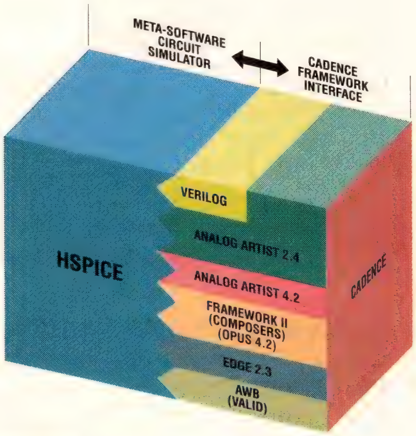
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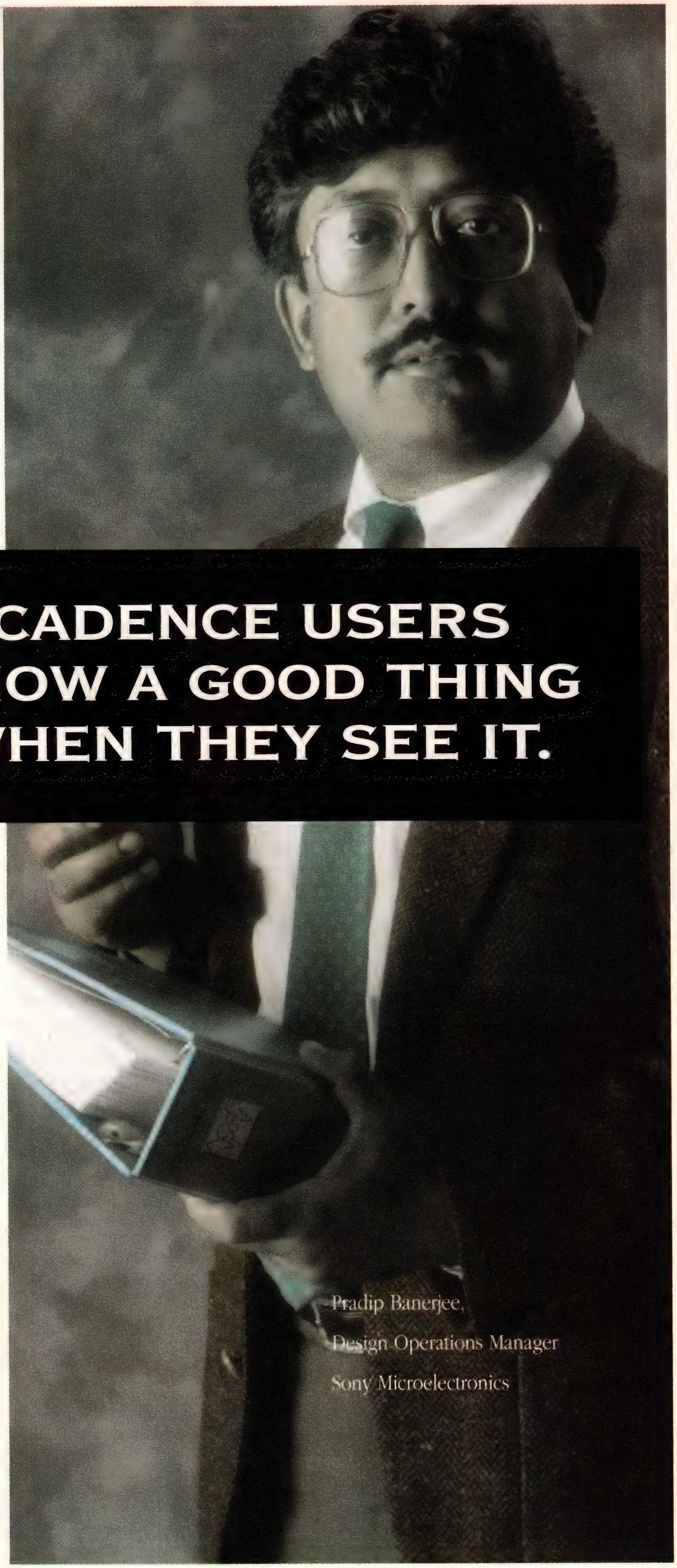

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CIRCLE NO. 87

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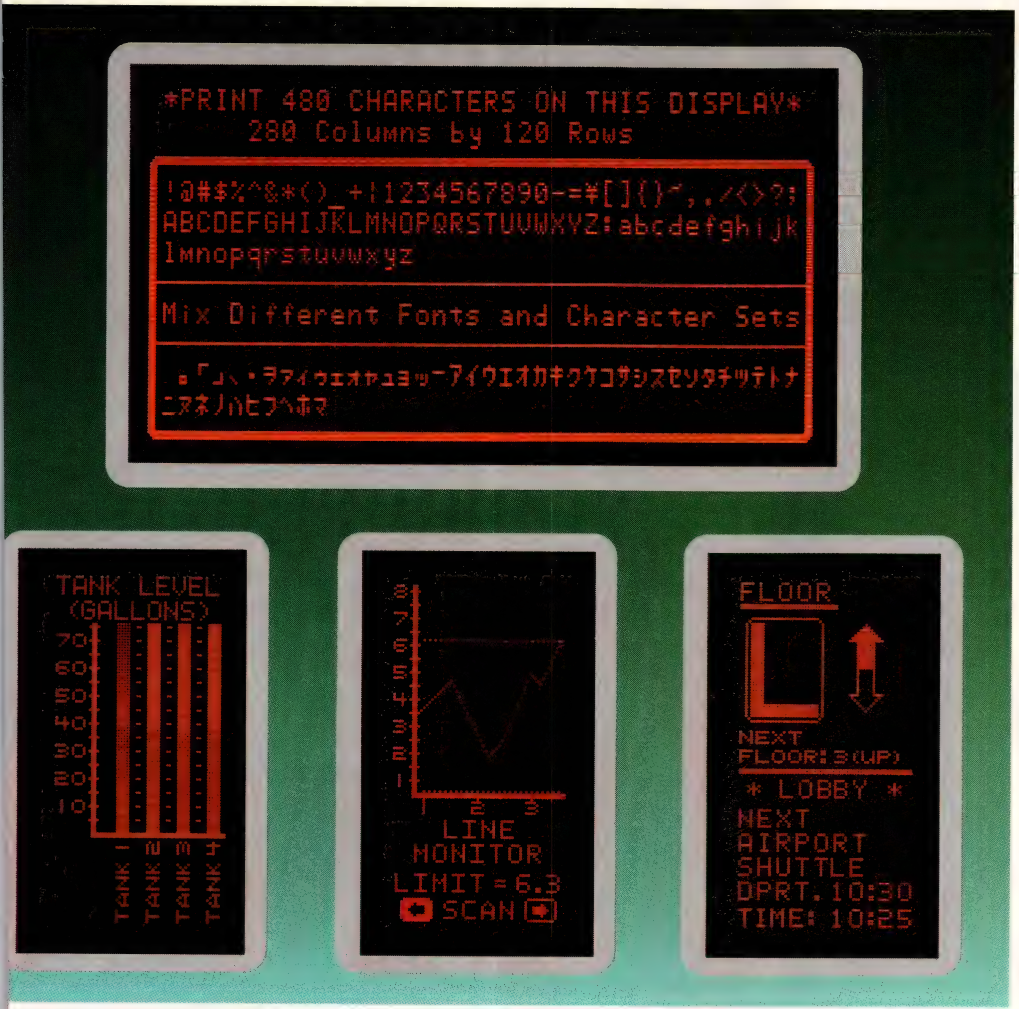

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A full-field, dot matrix, gas plasma, flat panel display with bright, neon orange pixels and a wide (130°) viewing angle that can display text and graphics - or both.

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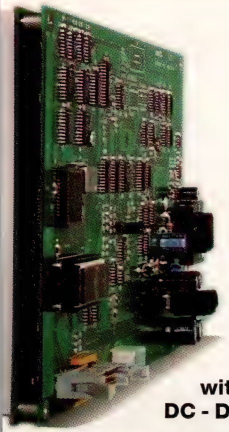
The Plasmadot concept is a natural for custom designs in terms of glass size, resolution, icons or electronics. Call or write today for complete specifications. Remember, if you're looking for a new display solution, put a Cherry in your picture.



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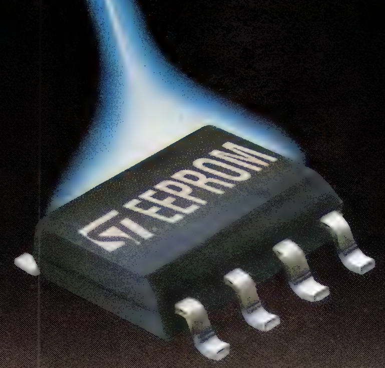

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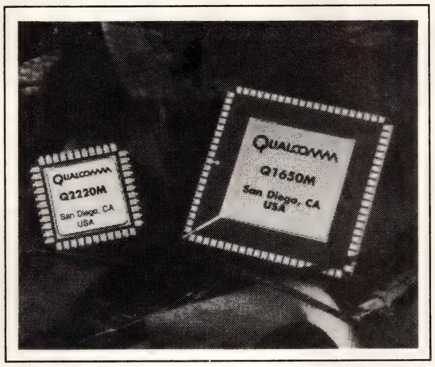
EDN 2/4/93

**Embedded controller.** The H8/510 ROMless embedded controller runs on a 3V supply. It operates at 5 MHz and has a minimum instruction time of 400 nsec. The device features a 16-bit data bus and a 16-Mbyte external memory-address space. You develop programs using a high-level language, which the CPU directly executes. The chip includes a 16-bit timer, two serial channels, and a 10-bit A/D converter. $12 (100). **Hitachi America Ltd,** 2000 Sierra Point Pkwy, MS-080, Brisbane, CA 94005. Phone (800) 285-1601, ext 21; (415) 589-8300. FAX (415) 583-4207.
**Circle No. 435**

**Digital radio transceiver.** The TR-1 1.8×2.2-in. card contains a 2-way radio for wireless transmission of digital data. The radio operates from 902 to 928 MHz and employs amplitude modulation. The transceiver is half duplex and reaches distances of 50 ft indoors. It achieves data rates of 2.4 kbaud and comes with an FCC certification. $160. **Kiefer Electronic Development,** 1727 Hawthorn Pl, Boulder, CO 80304. Phone (303) 444-2535. FAX (303) 444-7709.
**Circle No. 436**

**RF power transitor.** The MRF157 is an all-gold 600W RF power transistor. When operating with a 50V power supply, typical characteristics include 20-dB gain at 30 MHz, 45% drain efficiency, and third-order intermodulation distortion of −25 dB at the rated power output. $499. Delivery, stock to 16 weeks. **Motorola Inc—E 114,** 5005 E McDowell Rd, Phoenix, AZ 85008. Phone (602) 244-3818. FAX (602) 244-4597.
**Circle No. 437**



**DDS and Viterbi codec.** The Q2220M-40L is a direct digital synthesizer (DDS), and the Q1650M-2L is a Viterbi codec (encoder/decoder). The DDS can operate at a 40-MHz clock rate and has a minimum delay of 5 clock cycles. An on-chip sine-wave function has a 10-bit resolution and the spurious levels are below −60 dBc. The Viterbi codec implements 1/3, 1/2, 3/4, and 7/8 code rates. The chip also has CCITT V.35 data scrambling and bit-error-rate monitoring. Both chips operate from −55 to +125°C. **Qualcomm,** 10555 Sorrento Valley Rd, San Diego, CA 92121. Phone (619) 597-5005. FAX (619) 452-9096.
**Circle No. 438**

**Floppy-disk controller.** The 82078 is a floppy-disk controller for 3.3V systems. The unit is based on the company's 82077AA/SL chip and features a power-down mode that consumes less than 50 μA. It also features a 16-byte FIFO buffer and a high-speed host interface to permit its use in multimaster architectures such as the EISA or Micro Channel Architecture bus. The chip comes in a 64- or 44-pin quad flatpack. $4 to $6. **Intel,** Literature packet #HP-59, Box 7641, Mt Prospect, IL 60056. Phone in US and Canada, (800) 548-4725.
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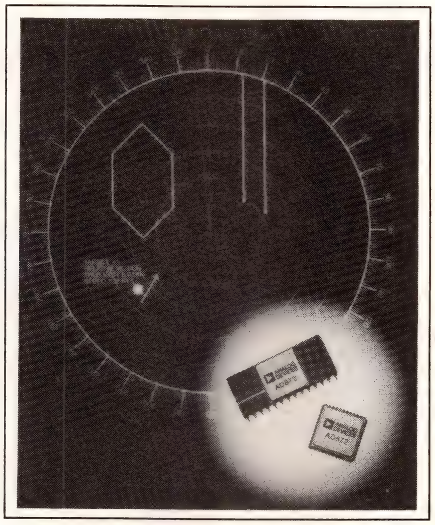
**Full-duplex modem.** The CMOS FX469 is a full-duplex pin-selectable 1200- or 2400-baud fast FSK (frequency-shift-keying) modem. Mark/space frequencies are 1200 and 1800 Hz, and 1200 and 2400 Hz on 1200- and 2400-baud selections, respectively. Tone frequencies are phase continuous, and transitions occur at zero crossing point. The IC needs an external 1.008- or 4.032-MHz crystal. CMOS FX469 chip in 20-pin SOIC, 22-pin ceramic DIP, 24-pin plastic quad flatpack, or 24-pin plastic leaded chip carrier, £5.47 (1000). **Consumer Microcircuits,** Witham CM8 3TD, UK. Phone 376-513833. FAX 376-518247. **Circle No. 440**

In US, **MX-COM Inc,** Winston-Salem, North Carolina. Phone (919) 744-5050. FAX (919) 744-5054. **Circle No. 441**

**Power amplifier.** The TDA7294 power amplifier outputs 50W rms continuously with 0.5% max total harmonic distortion (THD) over 20 Hz to 20 kHz. THD is typically 0.005% with 5W output at 1 kHz. The IC includes mute and standby functions (requires 1 mA typically), and short-circuit and thermal overload protection. The multiwatt 15-lead plastic package has a junction-to-case thermal resistance of 1.5°C/W max. $5 (10,000). **SGS-Thomson Microelectronics,** 20041 Agrate Brianza, Italy. Phone (39) 6031. FAX (39) 603-5555. **Circle No. 442**



**12-bit ADC.** The AD872 monolithic 12-bit A/D converter operates at 10M samples/sec. It includes a differential input track-and-hold amplifier and a voltage reference. The signal-to-noise plus distortion ratio is 65 dB at 1 MHz, and the differential nonlinearity is typically ½ LSB. The chip dissipates 1.15W and comes in a 28-pin DIP or 44-pin LCC. From $165. **Analog Devices Inc,** 181 Ballardvale St, Wilmington, MA 01887. Phone (617) 937-1428. FAX (617) 821-4273. **Circle No. 443**

**4-Mbit DRAMs.** The HM51S4800A/AL and HM51S4260A/AL 4-Mbit dynamic RAMs (DRAMs) have 512k×8-bit and 256k×16-bit organizations, respectively. One feature lets you place the DRAMs in a self-refresh mode by bringing the RAS line low for 100 μsec. Because the chips are internally refreshed, you can put the rest of the system to sleep by turning off the system clock. The refresh interval is 125 μsec instead of the standard 15.6 μsec. The 80-nsec version of the 512k×8-bit DRAM, $21; the 80-nsec version of the 256k×16-bit DRAM, $25 (100). **Hitachi America Ltd,** Semiconductor & IC Div, 2000 Sierra Point Pkwy, MS-080, Brisbane, CA 94005. Phone (800) 285-1601, ext 11; (415) 589-8300. FAX (415) 583-4207. **Circle No. 444**

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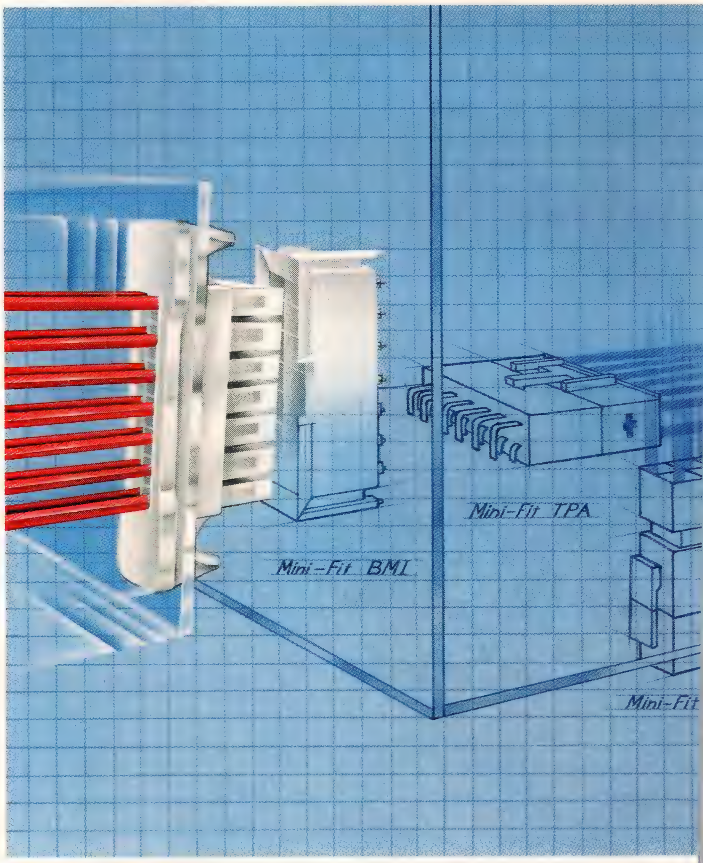

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CIRCLE NO. 91

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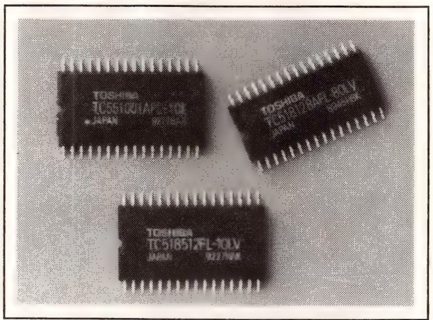
**Nonvolatile RAMs.** The Autostore family of NovRAMs automatically stores and recalls between static RAM (SRAM) and onboard shadow EEPROM without intervention by the host CPU. The feature saves the contents of the SRAM in the shadow EEPROM whenever the voltage to the chip falls below a preset level. Store operation takes 2.5 msec or less, and recall takes 10 µsec or less. Commercial X20C16P, $9.75 (1000). **Xicor Inc,** 1511 Buckeye Dr, Milpitas, CA 95035. Phone (408) 432-8888. FAX (408) 432-0640. **Circle No. 445**

**SCSI active terminator.** The REG1117 2.85V regulator provides an active termination for the SCSI-2 bus. You can use the chip for either standard, 18-line, or wide, 27-line, SCSI buses. One advantage of the active over a passive termination is that the quiescent power reduces from 1W to 50 mW. In addition, cable-impedance matching permits data rates as fast as 10 Mbytes. $1.85 (1000). **Burr-Brown Corp,** Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. FAX (602) 889-1510. **Circle No. 446**

**Video amplifiers.** The LT1187 and LT1189 monolithic video amplifiers have 50- and 35-MHz bandwidths, respectively. They detect differential signals and convert them to single-ended outputs. Typical common-mode rejection ratio is 100 dB. Both amplifiers have a 20-mA output drive current. They can run on 5V, ±5V, or ±8V power supplies. From $2.95 (100). **Linear Technology Corp,** 1630 McCarthy Blvd, Milpitas, CA 95035. Phone (408) 432-1900. **Circle No. 447**

**Battery charger.** The DS1633 smart charger can charge batteries without the need for external components. Optimized for 3V systems, the unit can charge one to three NiCd-cell battery pack or a single rechargeable 3V lithium cell at a maximum current of 100 mA. The unit charges the battery at maximum current until it exceeds a preset limit. $2.90 (5000). **Dallas Semiconductor,** 4401 S Beltwood Pkwy, Dallas, TX 75244. Phone (214) 450-0448. **Circle No. 448**

**3V SRAMs.** A series of 3V static RAMs (SRAMs) and 3.3V pseudo SRAMs (PSRAMs) are available. The family consists of a 256-kbit SRAM having a 32k×8-bit organization; a 1-Mbit SRAM having a 128k×8-bit organization; a 1-Mbit PSRAM having a 128k×8-bit organization; and a 4-Mbit PSRAM having a 512k×8-bit organization. The devices provide a 40% power savings over similar 5V devices. Access times range from 150 to 200 nsec. $6.50 to $21.50 (100). Delivery, 12 to 14 weeks ARO. **Toshiba America Electronic Components Inc,** 9775 Toledo Way, Irvine, CA 92718. Phone (714) 455-2000. **Circle No. 449**



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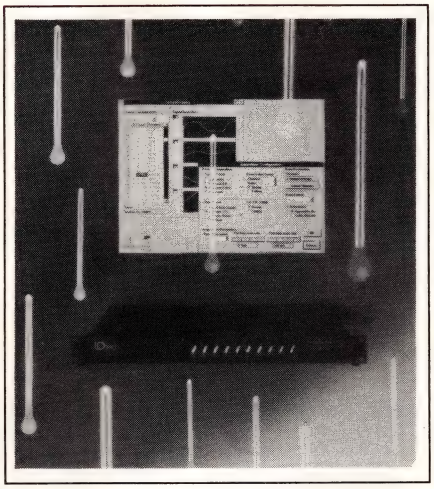
CIRCLE NO. 92

**Real-time spectrum analyzer.** The 3054 DSP system uses a bank of filters (implemented in a DSP μP) to provide spectral frame update rates as fast as 12.5 μsec. The system covers 100 Hz to 100 MHz and stores data covering periods as long as 26,000 sec. You can select transforms having from 32 to 1024 frequency bins and display from 26 to 801 of them; and, you can choose a power or phase display. You can tune to any center frequency from dc to 10 MHz and view the region around it with expanded resolution. A spectrogram mode displays multiple spectra with amplitude represented by color. $126,950. Delivery, six weeks ARO. **Tektronix Inc,** Box 4495, MS 38-386, Beaverton, OR 97076. Phone (800) 835-9433.
**Circle No. 401**

**Temperature-measurement system.** The 1.75-in.-high Tempscan/1000 mounts in EIA racks and scans 32 thermocouples, linearizing their outputs, and providing cold-junction compensation. It also handles thermistors and resistance-temperature detectors. The unit, which uses a 16-bit 200k-sample/sec ADC, permits expansion to 992 channels by adding 32- or 64-channel slave units that have dimensions equal to those of the master. The unit has IEEE-488 and RS-232C/RS-422 interfaces. It also has 32 programmable alarm outputs. The accompanying software, which controls the system setup, runs under MS-Windows. $1995. Delivery, eight weeks ARO. **IOtech Inc,** 25971 Cannon Rd, Cleveland, OH 44146. Phone (216) 439-4091. FAX (216) 439-4093.
**Circle No. 402**



**VMEbus simultaneous sample/hold ADC board.** The DVME-630F single 6U-size VMEbus board continuously and simultaneously samples two analog channels with 12-bit resolution at 2M samples/sec/channel and processes the data in a 32-MHz TMS320C30 DSP μP. When you acquire only one channel, the DVME-630F will interleave the operation of its two samplers to capture 4M samples/sec. The continuous acquisition capability results from using a 512-kbyte high-speed dual-ported RAM (expandable to 1.5 Mbytes) and a very-high-speed 8k × 32-bit expansion RAM. Board prices, from $5495; 1-Mbyte expansion module for the dual-ported RAM, $1195; executive software, $495; full source code for the software, $1195. **Datel Inc,** 11 Cabot Blvd, Mansfield, MA 02048. Phone (508) 339-3000, ext 123. FAX (508) 339-6356. **Circle No. 403**

**i486-based ISA bus data-acquisition board.** The DAP 3200e full-length board for the 16-bit ISA bus includes an i486SX μP and either 1 or 4 Mbytes of RAM. A multitasking real-time operating system, DAPL V4.0, resides on the board. With external expansion

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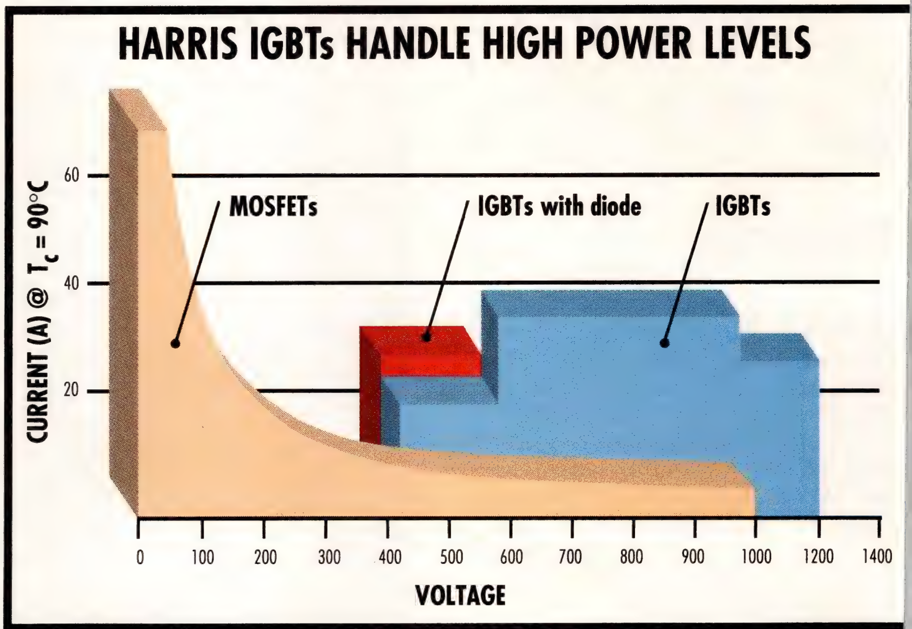

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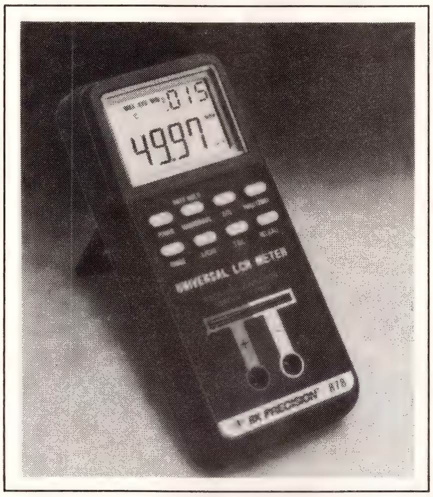
hardware, the board can sample 512 analog and 128 digital inputs at a combined rate of over 4M samples/sec while simultaneously processing the acquired data and updating 66 analog and 128 digital outputs. Dual 512-word FIFO buffers allow the board to bypass DMA hardware. From $3495. **Microstar Laboratories,** 2265 116th Ave NE, Bellevue, WA 98004. Phone (206) 453-2345. FAX (206) 453-3199. **Circle No. 404**

**Video line selector.** The 1.5×2.25×5.25-in. 6030 is a battery-powered accessory that gives almost any scope capabilities normally found only in laboratory scopes. Using a push-wheel switch, you can view any line of a 525-line National Television Standards Committee signal or a 625-line signal. A user-programmable switch position allows the unit to accommodate nonstandard TV formats to 1999 lines per frame, with scanning frequencies from 15 kHz to 64 kHz. A pair of BNC connectors allows loop-through of 75Ω signals. $299; NiCd battery option, $50. **Dumont E&R Electronics Inc,** 323 New Rd, Parsippany, NJ 07054. Phone (201) 575-8666. **Circle No. 405**



**Handheld LCR bridge.** The 878 measures inductance (L) from 0.1 μH to 2000H, capacitance (C) from 0.1 pF to 10,000 μF, and resistance (R) from 0.1Ω to 20 MΩ, with a basic error limit of 0.7%. Its LCD's two displays can simultaneously indicate capacitance and dissipation factor or inductance and quality factor (Q). The unit can provide an audible indication when a component value is outside programmable limits. A min/max function keeps track of the highest and lowest values measured. $275. **B+K Precision Div of Maxtec International Corp,** 6470 W Cortland St, Chicago, IL 60635. Phone (312) 889-1448. **Circle No. 406**

**Software libraries for MS-DOS and MS-Windows.** PCI-20369S-1 linkable library software allows the development of data-acquisition applications that run under MS-Windows V3.x. The software supports analog sampling at rates to 1M sample/sec. The library also provides a consistent interface between popular programming languages and the vendor's data-acquisition hardware. $295; free with the vendor's PCI-20501C, PCI-20098C, and PCI-20377W-1 boards. Upgrades from earlier versions of the library, $95. **Intelligent Instrumentation,** 6550 S Bay Colony Dr, MS 131, Tucson, AZ 85706. Phone (800) 685-9911; (602) 573-0887. FAX (602) 573-0522. **Circle No. 407**

**Handheld DMM.** The dual-display DM-7100 provides 19 functions, 29 ranges, and 3¾-digit resolution. It

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|---|---|---|---|
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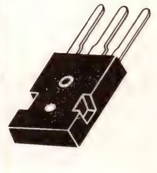
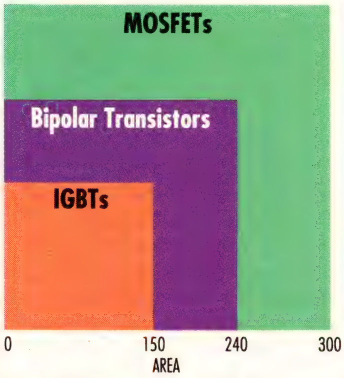
| HGTG20N120E2 | 20A | 1200V | TO-247 |
| HGTG12N60D1D | 12A | 600V | TO-247* |
| HGTG24N60D1D | 24A | 600V | TO-247* |
| HGTG32N60E2 | 32A | 600V | TO-247 |
| HGTD6N50E1 | 6A | 500V | TO-251 |
| HGTD6N50E1S | 6A | 500V | TO-252 Surface Mount |
| HGTP10N50C1 | 10A | 500V | TO-220 |

*with anti-parallel diode



Harris IGBTs are available with or without diodes in standard 3-lead packages.

ONE-QUARTER THE DIE SIZE



For applications at 500V and higher, Harris IGBTs require less silicon area than MOSFETs of equivalent current, voltage and Rds(on) characteristics. This equates to lower cost as compared to MOS.

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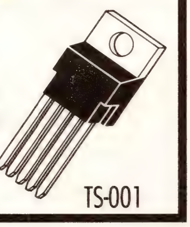
| • Turn Off | Turns off when gate drive is removed. |
| • On-State Voltage Drop | Nonlinear. Like that of an SCR/MCT. Temperature independent. Unlike the typical 2X variation of a power MOSFET. |
| • Turn-On Speed | Fast! Comparable to a standard power MOSFET. |
| • Turn-Off Speed | Comparable to a bipolar transistor. |



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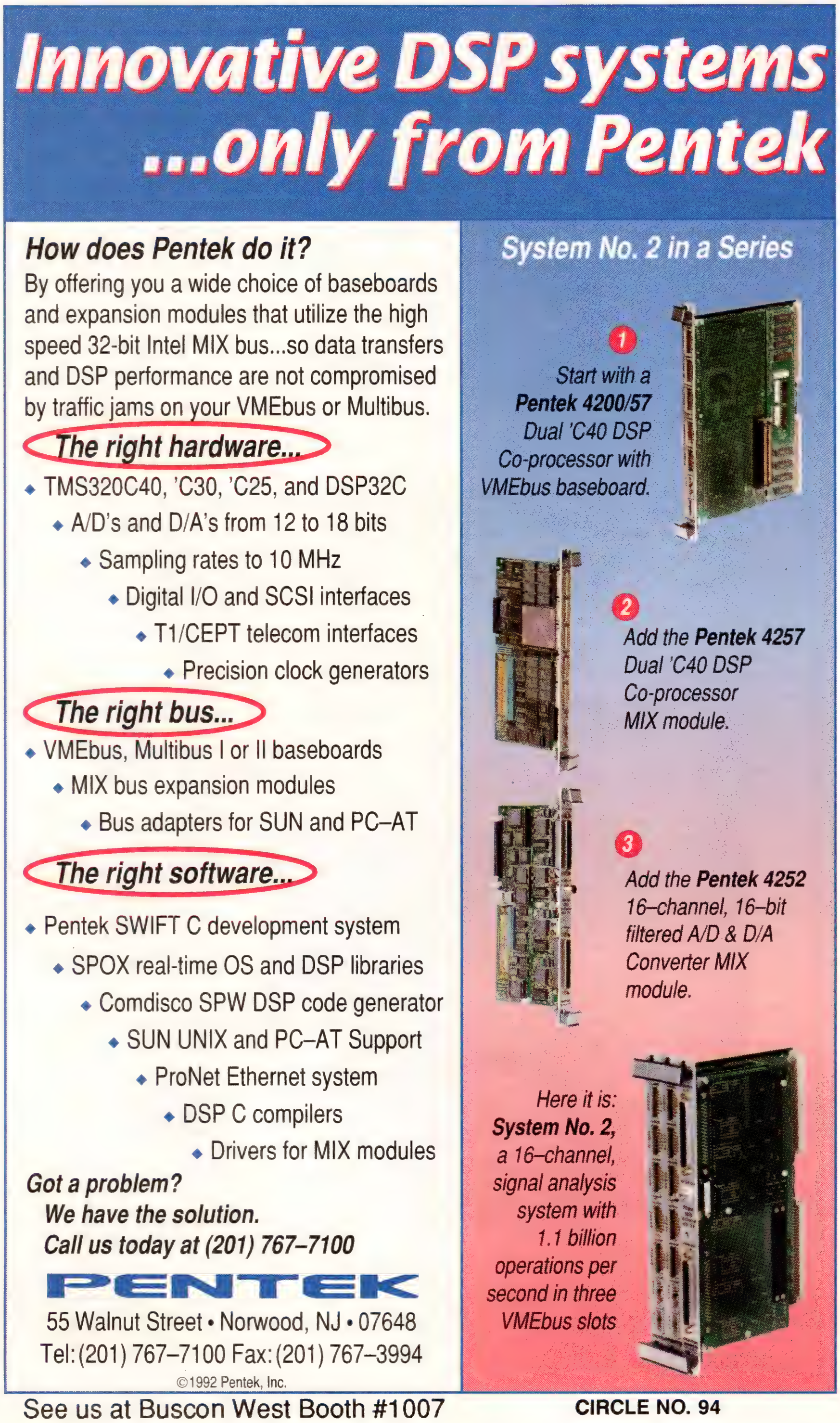
measures dc volts on five ranges from 400 mV to 1 kV full scale; ac volts on four ranges from 4 to 750V full scale; dc and ac current on two ranges each (400 mA and 4A full scale); resistance on six ranges from 400Ω to 40 MΩ full scale; frequency from 10 to 200 kHz; and capacitance from 4 nF to 40 µF full scale. The dual display can indicate ac voltage and frequency simultaneously. $149.95. **A W Sperry Instruments Inc,** 245 Marcus Blvd, Hauppauge, NY 11788. Phone (516) 231-7050. **Circle No. 408**

**Enhanced handheld DMM/DSOs.** The 93, 95, and 97 Scopemeters have additional measurement and display functions. Among them are a percent duty-cycle mode, a low-resistance range with $10^{-2}\Omega$ resolution, higher resolution in the frequency-counter mode, and the ability to invert waveforms on both channels and to time-stamp minimum and maximum values. $1350 to $1950. All units now being shipped include the enhanced features. Owners of existing units can have them upgraded for $155 by returning them to the manufacturer. **John Fluke Mfg Co Inc,** Box 9090, Everett, WA 98206. Phone (800) 443-5853; (206) 347-6100. FAX (206) 356-5116. TWX 910-445-2943. **Circle No. 409**
**Philips Test and Measurement,** Bldg TQIII-4, 5600 MD Eindhoven, the Netherlands. Phone local office. **Circle No. 410**

**50-MHz i486 DX2- and 20-MHz 486SLC-based VXI controllers.** The VXIpc-486 Model 200 series (from $3995) and Model 500 series (from $5595) are based on the 20-MHz Cx 486SLC (with optional math coprocessor) and the 50-MHz i486 DX2, respectively, µPs. These controllers replace the vendor's earlier i386-based VXI controllers. Both series include 1-, 2-, and 3-slot C-size units with as much as 16 Mbytes of RAM. The 1-slot models include an 80-Mbyte hard disk; the 2-slot units add a 3½-in. floppy-disk drive and have hard-disk capacity to 240 Mbytes; and the 3-slot units have hard disks that store as much as 426 Mbytes. **National Instruments Corp,** 6504 Bridge Point Pkwy, Austin, TX 78730. Phone (800) 433-3488; (512) 794-0100. FAX (512) 794-8411. **Circle No. 411**

**VXIbus waveform digitizers.** The E1413A ($5900) acquires 100k samples/sec with 16-bit resolution. The E1427A ($11,800) acquires 2G samples/sec with 7-bit resolution. The E1430A ($12,000) captures 10M samples/sec with 18-bit linearity. The E1485A ($10,500) is a digital signal processor for use with digitizers such as the E1430A that can transfer data via the VXI local bus. Delivery, four to six weeks ARO. **Hewlett-Packard Co,** Box 58059, MS 51L-SJ, Santa Clara, CA 95051. Phone (800) 452-4844. **Circle No. 412**

**Notebook-PC-based optical time-domain reflectometer.** The COM-1020 is based on the vendor's FCS-100 card. The vendor describes the instrument as waterproof and capable of withstanding the most severe abuses it might be subjected to in the field. The unit, which with optional batteries operates from four to eight hours without ac power, can store thousands of traces and can transfer them via modem. The pull-down, menu-based software minimizes the need for operator training. $995. **Exfo EO Engineering Inc,** 465 Godin, Vanier, PQ G1M 3G7, Canada. Phone (418) 683-0211. FAX (418) 683-2170. **Circle No. 413**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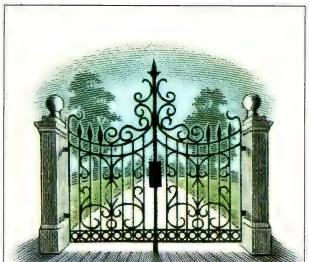
# *The* REMARKABLY DENSE ARGUMENT FOR THE CROSSPOINT FPGA.



**10,000**
*useable gates on one 12K chip.*

**Field Programmable Gate Arrays have always been a promising sort of product. But they haven't had nearly enough useable gates. Not to mention their pitifully low performance. And as a**

*fig.* 1

**The Real World**

*It's a nasty, demanding place. Now there's an* FPGA *with enough density to let you build the mainstream products that are used in it.*

**result, the ASIC designer has seldom bothered with them. The Crosspoint FPGA is**

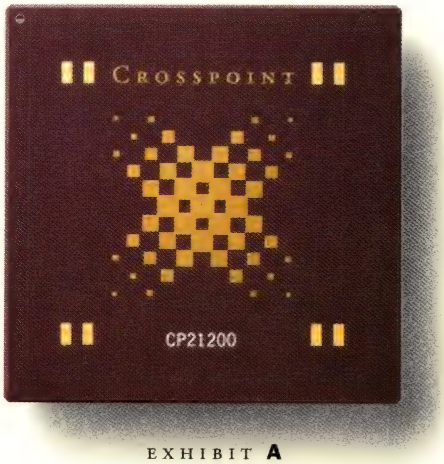


EXHIBIT **A**
*The product. In through-hole.*

**a dream product that breaks all this wide open. It offers up to 10,000 true, useable gates on one 12K chip, and it's fast. Will it change design permanently?**

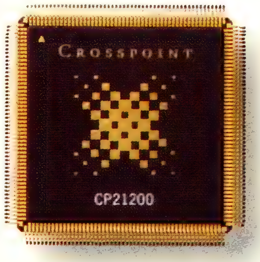


EXHIBIT **B**
*The product. In surface mount.*

**We submit that it will.**

**In name, it's a 12K. But it gives you far more useable gates than that suggests. It's also fast. And predictable. All in all, a lot like a gate array. There's a reason.**

# IT *Is* A GATE ARRAY

Crosspoint gives you the industry's first 12K FPGA. But there's considerably more to it than that.

And, at the same time, less.

The Crosspoint FPGA offers unheard-of gate-utilization efficiency. The highest-available FPGA performance. And remarkable predictability with both.

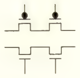


EXHIBIT **C**
*Simplicity itself: our gate.*

All for one simple reason. Unlike *all other* FPGAS, Crosspoint's is—architecturally—a gate array.

Like a mask-programmable gate array, it has transistor-level granularity. And unlike previous FPGAS, it has gates.

Which, in itself, is noteworthy.

The smallest building blocks of all previous FPGAS are elaborate and complicated constructions—incorporating numerous logic macrocells with numerous functions. And resulting in an extremely complex chip for a rather modest number of "gates."

The smallest building block of the Crosspoint FPGA is something far simpler—a gate. A real one.

And that, in turn, is why our "12K" chip actually is a 12K—and gives you up to 10,000 useable gates— 10,000 *true,* gate-array gates. Which is a gate-utilization efficiency of up to 85%. Efficiency comparable to that of other true gate arrays. And, of course, far in excess

Crosspoint Solutions Incorporated

of what you get from existing FPGAs.

Our superior *performance* is also due to our streamlined architecture. We function in systems with clock speeds up to 50 Mhz. Which may not seem altogether meaningful in the murky environment of FPGA performance claims. But is very meaningful when you consider that *other* FPGAs will only function in systems in the 15-30 Mhz range.

*fig.* 2

**Duck**

*There's an old saying: If it looks like a duck, and acts like a duck, it must be a duck. Our* FPGA *acts like a gate array, and is one.*

The *predictability* of the Crosspoint FPGA is significant in itself. As with a gate array, you'll know what size circuit you can fit on the chip, and what speed it will operate at. So you'll know you aren't just spinning your wheels.

And we also give you built-in testability logic, per the JTAG Boundary Scan Architecture Standard—which will make board testing painless, and assure high quality.

At a glance, that's what the product is — technically.

What it *means,* is that for the first time you've got the FPGA you need. One without limitations, that will let you use FPGAs where you'd like to. In real-world products.

**We'll also give you something else you can only get with a true gate array (and we think you'll especially appreciate our tools).**

# THE POWER *of* LOGIC SYNTHESIS.

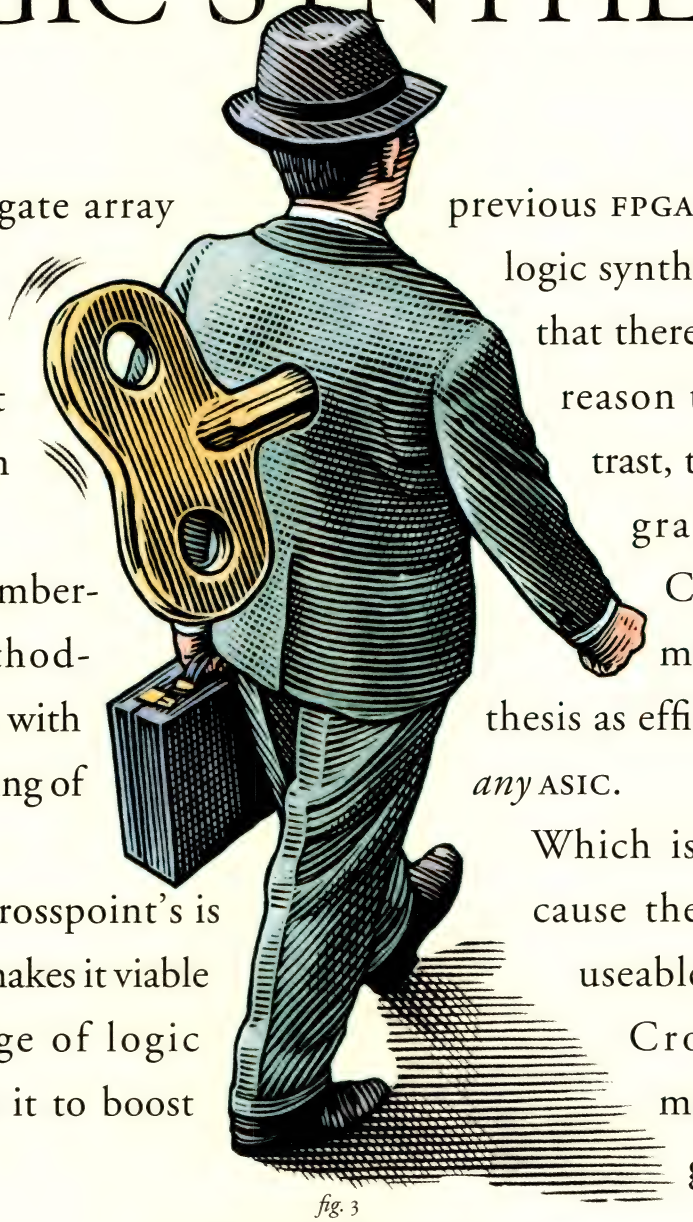


*fig. 3*

**Your Own Automated Designer**

*You don't have to use logic synthesis, but there's a good reason to. Productivity. It's like having a clone of yourself. He excels at details and will go right where you point him.*

Because of its gate array architecture, the Crosspoint FPGA is a perfect fit in the ASIC design environment.

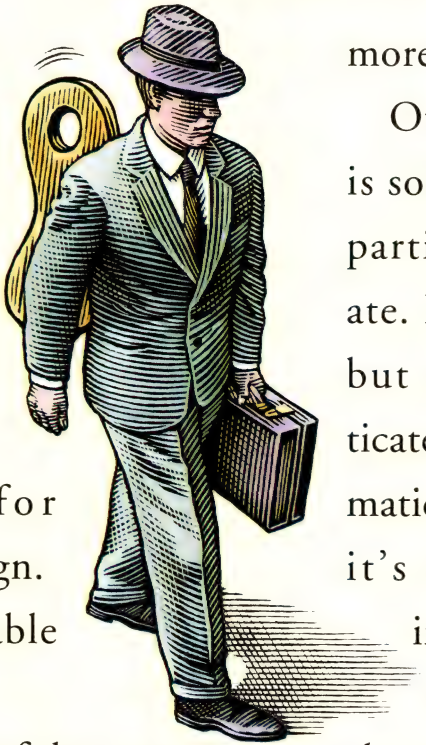
It makes the cumbersome design methodology you associate with FPGAs, entirely a thing of the past.

For instance, Crosspoint's is the first FPGA that makes it viable to take advantage of logic synthesis, and use it to boost productivity.

The coarse granularity of previous FPGAs has made *using* logic synthesis so inefficient that there's been very little reason to do it. By contrast, the transistor-level granularity of the Crosspoint FPGA makes logic synthesis as efficient as it is with *any* ASIC.

Which is significant, because the extremely high useable-gate count that Crosspoint offers means there are big gains to be realized *with* logic synthesis.

CROSSPOINT SOLUTIONS INCORPORATED



When it comes to the rest of design automation, you'll be able to use the tools you're familiar with. In precisely the ways you use them for standard ASIC design. And with predictable results.

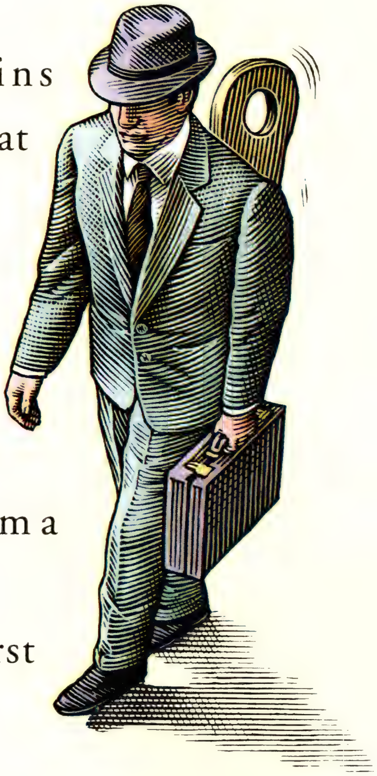
It is, in fact, one of the most important advantages we offer.

You'll find you can do both pre- and post-layout simulation. You'll have the familiar and efficient back-annotation path you expect with a gate array—something that's never previously been available for an FPGA.

And that will be true for any leading simulation product you work with. Crosspoint's Design Kits support the simulation, logic synthesis, schematic capture, and timing- and fault-analysis products of Mentor Graphics, Synopsys, Cadence / Verilog, Viewlogic. And more soon.

Our place & route is something you'll particulary appreciate. It not only *works,* but it's highly sophisticated. It's powerful, it's automatic, it's flexible, it's timing-driven, it's intuitive. And it offers an interactive editing capability that will help you fine-tune, if you choose to.

All in all, we've been careful to give you the tools that will make it not only feasible, but *easy* to realize the major gains that the Crosspoint FPGA allows for.



But those gains themselves are what matter most.

The sorts of density, performance, predictability—in fact *everything*—that you expect from a gate array.

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CROSSPOINT SOLUTIONS INCORPORATED

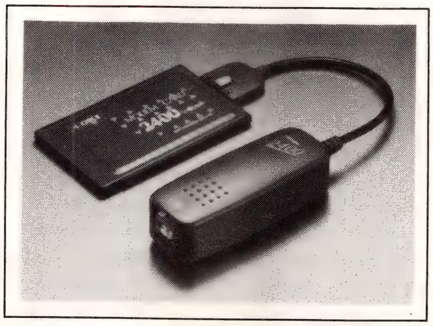
5000 *Old Ironsides Drive, Santa Clara, California* 95054 *Telephone* 408 988.1584 *Fax* 408 980.9594

**3-Gbyte disk drive.** The Model 1936 family of 5¼-in. disk drives provides 3.6 Gbytes of unformatted data capacity and data-transfer rates as high as 20 Mbytes/sec. The family includes an 8-bit Fast SCSI-2 model with single-ended SCSI interface; an 8-bit Fst SCSI-2 model with a differential SCSI interface; a 16-bit Wide Fast SCSI-2 model; and a concurrent dual-port Wide Fast SCSI-2 model. $4895 to $5195. **Micropolis Corp,** 21211 Nordhoff St, Chatsworth, CA 91311. Phone (818) 709-3300. FAX (818) 709-3497. **Circle No. 450**

**Rugged 1.8-in. disk drives.** The Miniport 42 and Miniport 85 1.8-in. disk drives provide 42 and 85 Mbytes of storage, respectively, and withstand 200g shocks, even while operating. They're available with either PCMCIA (Personal-Computer, Memory-Card International-Association) or IDE interfaces. The PCMCIA version contains a PCMCIA controller that includes attribute memory. It allows a PCMCIA slot to accept other devices without the need for separate software drivers. 42-Mbyte sample, $350; 85-Mbyte sample, $545. **MiniStor Peripherals Corp,** 2801 Orchard Pkwy, San Jose, CA 95134. Phone (408) 943-0165. FAX (408) 434-0784. **Circle No. 451**

**VMEbus data-acquisition card.** The MPV961 2-channel, 12-bit ADC card samples as much as 25M samples/sec. You can program the card to sample in single-shot mode or in 500-sample/sec increments. Maximum input is ±1.024V, and system accuracy is ±2 LSB. The 32-Mbyte dual-port RAM enables the card to acquire and store data independently of host-processor intervention. The card includes a VSB interface, which you can use for programming and data transfer. You can order 20- or 25-MHz and single- or dual-channel versions. Dual-channel, 20-MHz version, £12,995. **Pentland Systems Ltd,** 1 Cochrane Sq, Brucefield Industrial Park, Livingston EH54 9DR, UK. Phone 506-464666. FAX 506-463030. **Circle No. 452**

**PCMCIA fax/modem cards.** PCMCIA modem cards provide fax/modem and data modem capabilities. Each is contained in a PCMCIA Type II package. Each operates from a 5V supply. The 2400-bps data-modem card draws 150 mW during power down, 225 mW during standby, and 550 mW during operation. The 9600-bps fax/modem card consumes 70, 300, and 750 mW, respectively, in those modes. Data modem, $300; fax/modem, $350 (100). **Oki Semiconductor,** 785 N Mary Ave, Sunnyvale, CA 94086. Phone (408) 720-1900. FAX (408) 720-1918. **Circle No. 453**



**PC accelerator card.** The RM04 PC-AT plug-in card improves speed of operation of computer-intensive applications by as much as 100×. It includes

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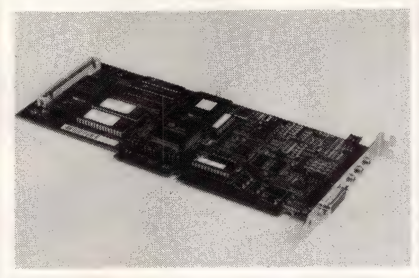
CIRCLE NO. 98

an i860 processor running at 25, 33, or 40 MHz, up to 72 Mbytes of dynamic RAM (DRAM), and a bidirectional 16-bit FIFO interface. The card also includes an Inmos Transputer link and subsystem control for multiprocessor networks. For system expansion, you can mount Transputer modules directly onto the card. RM04 with 25-MHz processor and 2-Mbyte DRAM, £2520. **Riverside Machines Ltd,** 20 Newmarket Rd, Cambridge CB5 8DT, UK. Phone 223-321083. FAX 223-321161. **Circle No. 454**

**Parallel-port multiplexer.** F/MUX lets you connect a variety of peripherals to your PC via the IEEE 1284 EPP enhanced parallel port. It accommodates printers, mass-storage devices, CD-ROM players, network adapters, and a variety of data links. The device is the size of a small power strip and connects to a PC's parallel port via a ribbon cable. 4-port model, $199; 8-port model, $249. **FarPoint Communications,** 104 East Ave K4, Suite F, Lancaster, CA 93535. Phone (805) 726-4420. FAX (805) 726-4438. **Circle No. 455**

**VAX accelerator.** The Vaccelerator AP/-40, a 100-MIPS add-in coprocessor for VAX and MicroVAX systems, runs VMS applications without modification. Using a 64-bit R4000 RISC processor, it increases MicroVAX performance by factors as high as 100 on standard industry benchmarks. As many as 10 boards can run in parallel in the same system. $9990. **Avalon Computer Systems,** 510 Castillo St, Santa Barbara, CA 93101. Phone (805) 965-9559. **Circle No. 456**



**Sound/speech board.** The Cyber Audio Card combines sound reproduction with speaker-independent speech recognition for multimedia PC systems. For speech recognition, the card keeps a 125-word vocabulary active and can download other words from disk. Its sound synthesizer uses actual samples of musical instruments rather than FM synthesis techniques. The card includes a MIDI (musical-instrument digital interface). $395. **Alpha Systems Lab,** 17912 Mitchell St, Irvine, CA 92714. Phone (714) 252-0117. FAX (714) 252-0887. **Circle No. 457**

**Graphics accelerator.** The SGX160 graphics accelerator, a 1-slot SBus board, works with the new Hitachi 21-in., 2M-pixel high-resolution, flat-screen monitor. It delivers 1600 × 1280 resolution at a 76-Hz refresh rate. The accelerator is register-level compatible with Sun's CG6 graphics standard. $3295. **Integrix Inc,** 1200 Lawrence Dr, Suite 150, Newbury Park, CA 91320. Phone (805) 375-1055. FAX (805) 375-2799. **Circle No. 458**

**Optical-disk integration kits.** The RF-SCSI kits for DOS, OS/2, Windows, and Novell Netware 386 environments include everything necessary to install

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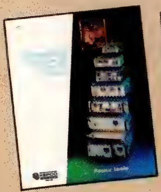
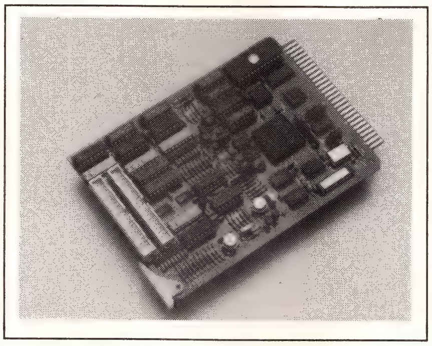


single or multiple optical drives. Each kit contains an adapter board, a device driver, software, a manual, and cable. The kits support all of the manufacturer's drives. Each installed optical drive appears to the system as a large-capacity hard drive. $325 to $995. **Plasmon Data Systems Inc,** 1654 Centre Pointe Dr, Milpitas, CA 95035. Phone (800) 445-9400; (408) 956-9400. FAX (408) 956-9444. **Circle No. 459**

**SBus port-expansion boards.** These SBus boards provide serial- and parallel-port expansion for Sun and SPARC-compatible workstations. In all, eight boards provide from 1 parallel port to 16 serial ports and combinations thereof. $175 to $1195. **Magma,** 6725 Mesa Ridge Rd, San Diego, CA 92121. Phone (800) 285-8990; (619) 457-0750. FAX (619) 457-0798. **Circle No. 460**

**80C51-based card for STD bus.** The MSI-C851 CMOS STD card, based on the 80C51FA controller, aims at embedded applications. It provides numerous memory and I/O functions and includes 64 kbytes of PROM and 128 kbytes of static RAM. Low-power idle and a power-down mode decrease power consumption. The card operates at 12 MHz and requires a single 5V supply. $316 (100). **Microcomputer Systems Inc,** 1814 Ryder Dr, Baton Rouge, LA 70808. Phone (504) 769-2154. FAX (504) 769-2155. **Circle No. 461**



**Sensor processor for STD bus.** The Model 7428/29 sensor-processor board for the STD bus operates in the temperature range of −40 to 85°C. It measures any combination of thermocouples, voltages, currents, RTDs, and strain and pressure gauges. Low power consumption (typically less than 3W) suits it for battery operation. $1075. **Sensoray,** 15800 Upper Boones Ferry Rd, Suite 150, Lake Oswego, OR 97035. Phone (503) 684-8005. FAX (503) 684-8164. **Circle No. 462**

**8-port fax board.** The 8-port Document Director PC fax board occupies a single PC/AT slot and works with OS/2 and Unix operating systems. As many as six boards can go in one computer; throughput ranges from 2400 bps to 14.4 kbps. $974 to $1374 per port. **OAZ Communications Inc,** 44920 Osgood Rd, Fremont, CA 94539. Phone (510) 226-0171. FAX (510) 226-7079. **Circle No. 463**

**Process-control-board computer.** The MP-11 single-board computer, based on the 68HC11F1, aims at process-control applications. The 4.5×5.5-in. board operates at 16 MHz and includes power and ground planes to minimize noise. An expansion connector allows use of an optional A/D and D/A daugh-

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voltage/current stabilization

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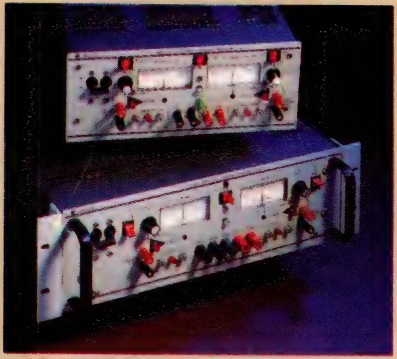

d-c four quadrant power
100-400 Watts
voltage/current stabilization

☐ Analog programmable, bandwidth to 20KHz ☐ Digitally programmable, built in GPIB or serial controller ☐ Precision stabilization: 0.001% source, 0.002% load

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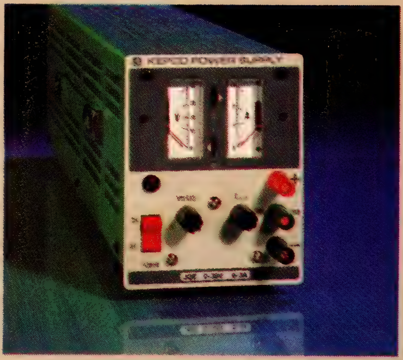

d-c single quadrant power
100-1000 Watts
voltage stabilization

☐ Analog programmable
☐ Precision stabilization:
0.0005% source, 0.005% load

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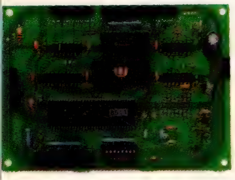
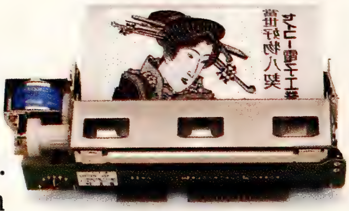


“ !” is all we hear. Okay, with one exception. Bill in Des Moines. He went through his new order sooner than expected and started yelling about getting more. Fast.

Noise like that we can easily quiet. Seiko Instruments has the broadest line of thermal printer mechanisms and stand-alone printers in the industry. Also the fastest.



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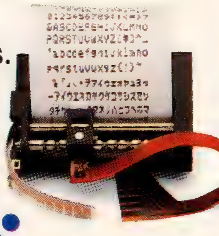


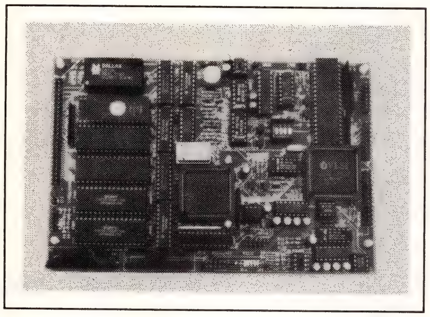
SII

Seiko Instruments

Seiko Instruments USA Inc
Electronic Components Division
2990 West Lomita Blvd., Torrance, CA 90505
Phone (310) 517-7787 Fax (310) 517-7792

CIRCLE NO. 97

ter board. Unpopulated bare board, $100; assembled and tested board, $300. **Allen Systems,** 2346 Brandon Rd, Columbus, OH 43221. Phone (614) 488-7122.
**Circle No. 464**



**Embedded control-board computer.** The Blue Jay single-board computer for embedded control has a built-in sound port that can play back speech and sounds. Measuring 5×7.5×0.6 in., the board consumes 1.5W of power. It has an 80C188 processor and includes an array of memory, communications, and user-interface features. From $395. **Bagotronix,** 1019 Crossing Brook Way, Tallahassee, FL 32311. Phone (904) 942-7905.
**Circle No. 465**

**VGA-compatible LCD module.** The 640×480 EG9013 LCD module is among the smallest available, measuring 124.6×194.8×8 mm. It's also suitable for use with an edge light, further contributing to a thin profile. It has a dot pitch of 0.20×0.20 mm and dot size of 0.17×0.17 mm. Its formulated nematic (FTN) technology achieves high contrast. Evaluation kit, $595. **Epson America Inc,** 20770 Madrona Ave, Torrance, CA 90503. Phone (310) 787-6300.
**Circle No. 466**

**Graphics controller.** The Harlequin 16-bit ISA bus graphics-controller card provides a TIGA interface to work with Windows, CAD, DTP, and multimedia applications. The card contains a 2-Mbyte video RAM and outputs in true color at 640×480- or 800×600-pixel resolution, or in 256 colors at 1280×1024-pixel resolution. Based on a 40-MHz TMS34020 processor, the card accommodates a 1- or 4-Mbyte dynamic RAM for TIGA support. The card works with PAL and NTSC modes, and a Windows 3.1 software utility provides ×8 zoom factor. £1195. **Datapath Ltd,** Alfreton Rd, Derby DE2 4AD, UK. Phone 332-294441. FAX 332-290667.
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Our 600 standard "Off The Shelf" DC/DC converters provide the performance, package style and price combination that will fit your application needs.

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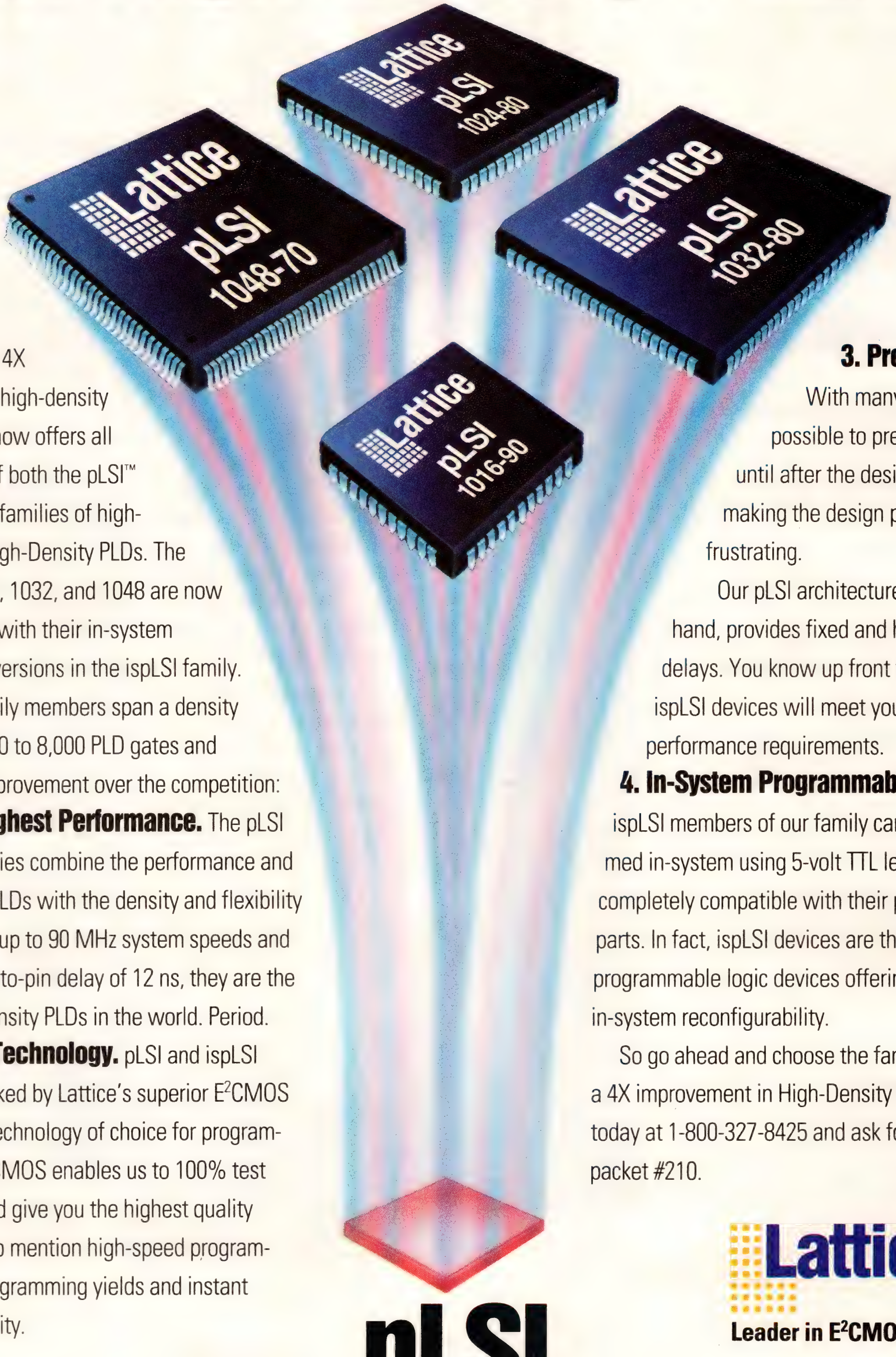

To achieve a 4X improvement in high-density design, Lattice now offers all four members of both the pLSI™ and the ispLSI™ families of high-performance, High-Density PLDs. The pLSI 1016, 1024, 1032, and 1048 are now available along with their in-system programmable versions in the ispLSI family.

The four family members span a density range from 2,000 to 8,000 PLD gates and provide a 4X improvement over the competition:

**1. World's Highest Performance.** The pLSI and ispLSI families combine the performance and ease of use of PLDs with the density and flexibility of FPGAs. With up to 90 MHz system speeds and a maximum pin-to-pin delay of 12 ns, they are the fastest High-Density PLDs in the world. Period.

**2. E²CMOS® Technology.** pLSI and ispLSI devices are backed by Lattice's superior E²CMOS process—the technology of choice for programmable logic. E²CMOS enables us to 100% test every device and give you the highest quality available. Not to mention high-speed programming, 100% programming yields and instant reprogrammability.

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**Leader in E²CMOS PLDs.**

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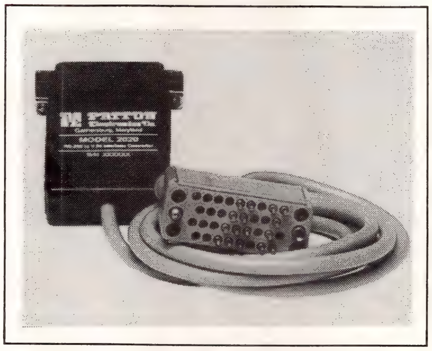
For Literature Circle No. 49

**5W DC-DC converter.** The NMX SO 5W dc/dc converters deliver single or dual outputs of 5, 12, or 15V. Input voltage is 5, 12, 24, or 48V. Models include 500V isolation, 0.5% line and load regulation, and current foldback short-circuit protection. Dimensions are 40×23×9 mm. Single-output converter, £20.91; dual-output converter, £22.90 (100). **Newport Components,** 4 Tanners Dr, Blakelands North, Milton Keynes MK14 5NA, UK. Phone (908) 615232. FAX (908) 617545. **Circle No. 468**

**Battery pack.** The C-LIFE CMOS backup battery has a useful life that exceeds 10 years. The unit contains a NiCd power pack and a special charging circuit tailored to the battery's characteristics. The unit derives power from a disk-drive power-output cable. Nominal output voltage is 4.25V. $25. **Clovis Point,** 215 Main St, Rochester, VT 05767. Phone (802) 767-9292. **Circle No. 469**

**N+1-redundancy switcher.** You can parallel up the outputs of six PK60-R 60W switching-mode power supplies to achieve n+1 redundancy operation. Single output is either 5V/12A, 12V/5A, 15V/4A, or 24V/2.5A. The switchers operate on 110 to 240V ac supplies. The switchers include output-diode protection to prevent reverse driving and open-collector outputs for unit isolation in the event of failure. 3U high module with 5-year warranty, £177 (50). **BICC-Vero Electronics,** Flanders Rd, Hedge End, Southampton SO3 3LG, UK. Phone (489) 780078. FAX (703) 264159. **Circle No. 470**

**80486-processor cooling fan.** You can mount this fan/heat-sink assembly directly onto an already socketed 486 chip using an integral stainless-steel saddle clip. The fan requires a 12V, 80-mA supply and runs at 5000 rpm. As an example, the assembly reduces the case temperature of a 25-MHz processor from 76 to 35°C. The fan has a minimum life of 30,000 hours. Overall size is 44×44×20.5 mm. £7.25(100). **Brookside Technologies,** Blairfordel, Kelty KY4 0HW, UK. Phone (383) 831528. FAX (383) 830192. **Circle No. 471**



**Interface converter.** Model 2020 lets a synchronous RS-232C host or terminal communicate with a DSU/CSU (data storage unit/circuit switching unit) incorporating a V.35 interface. It supports data rates of 200 kbps, communicates either full or half duplex, and is protocol independent. The device operates in either a DTE-to-DCE (Data Termination Equipment/Data Communications Equipment) or DCE-to-DTE mode. The unit has a male or female DS-25 connector on the RS-232C end and a male or female M/34 connector on the V.35 side. $295. **Patton Electronics Co,** 7958 Cessna Ave, Gaithersburg, MD 20879. Phone (301) 975-1000. FAX (301) 869-9293. **Circle No. 472**

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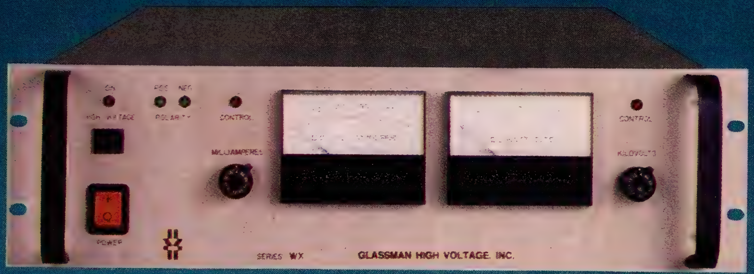

The 1000 watt Series WX offers well-regulated DC output voltage in ranges from 0 to 1 kV through 0 to 75 kV. Panel height is only 5.25 in. and weight less than 30 lbs. In addition to front panel control, the WX features remote monitoring and control, a TTL high voltage enable/disable, safety interlock terminals, and a +10 V external programming source.

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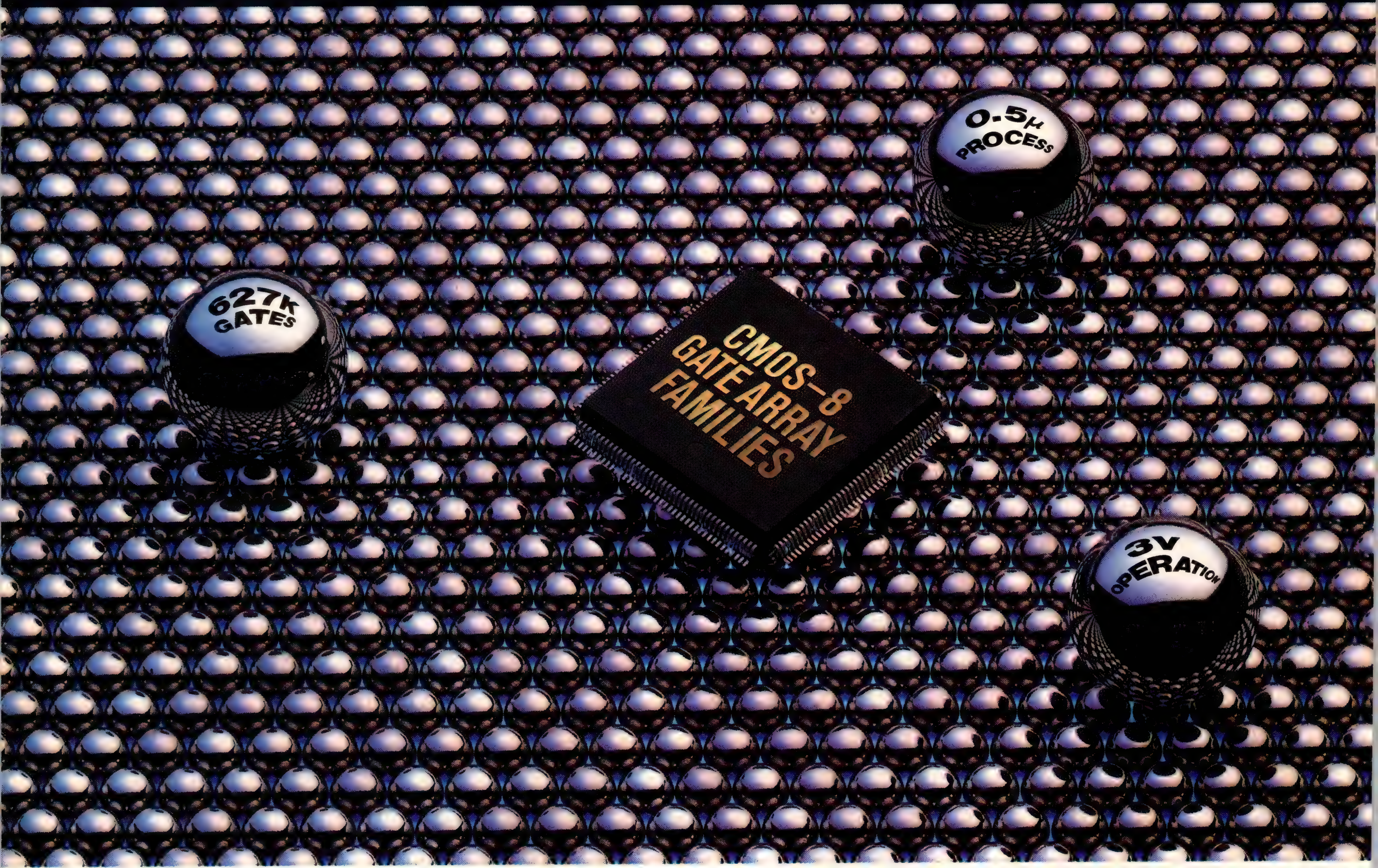

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NEC

CIRCLE NO. 127

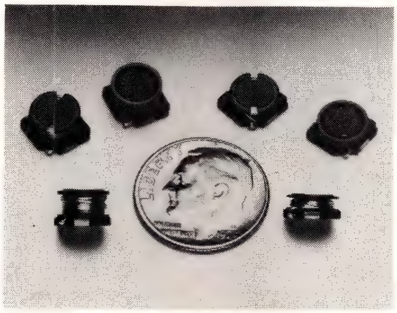
**Counters.** The Mini-Counter Series offers a choice of battery-operated rate meters, totalizers, quadrature meters, and a combination rate-meter/totalizer. All units are housed in a compact DIN size NEMA-4X enclosure. The units feature a 0.43-in.-high LCD readout and are easy to use. Setup and scaling is easily accomplished via the two front-panel pushbuttons. From $59. **Newport Electronics Inc,** 2229 S Yale St, Santa Ana, CA 92704. Phone (800) 639-7678; (714) 540-4914. **Circle No. 473**

**2.5V micropower reference.** The LM4431 bandgap reference outputs 2.5V ±2% with a typical TC of 30 ppm/°C at 25°C. The reference operates with drive current from 100 μA to 15 mA, and over 0 to 70°C ambient temperature range. Long-term stability is typically 120 ppm for 1000 hours at 25°C. SOT-23 package, $0.55 (1000). **National Semiconductor,** Raiffeisenstrasse 10, D-8016 Feldkirchen, Germany. FAX (89) 9033902. **Circle No. 474**

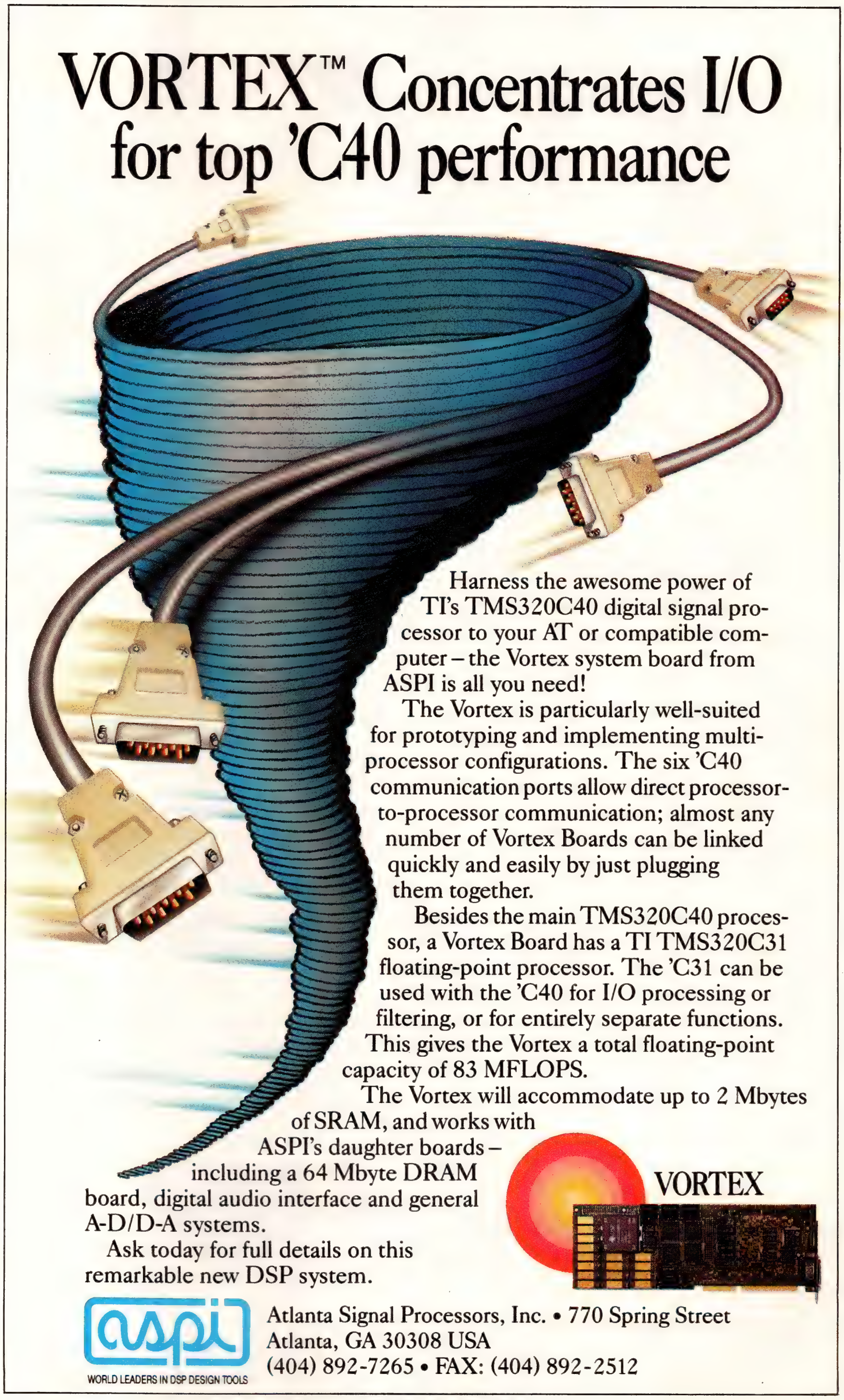
**Electrolytic capacitor.** Designed for switching power-supply applications, the Type TRS radial electrolytic capacitor operates over a −55 to +105°C range. Voltage ratings range from 6.3 to 63V, and capacitance tolerance equals ±20%. Maximum dissipation factors range from 0.09 $\tan\delta$ at 63V to 0.24 $\tan\delta$ at 6.3V. From $0.08 (1000). Delivery, stock to 10 weeks ARO. **Tecate Industries Inc,** Box 711509, Santee, CA 92072. Phone (619) 270-8707. FAX (619) 448-4811. **Circle No. 475**

**Resistor chip.** The TNPW1206 uses a specially developed protective coating to prevent electrolytic corrosion of the resistor's nickel-chromium element. The unit spans a 49.9Ω to 500-kΩ resistance range and has a ±25 ppm/°C standard temperature coefficient (±10 ppm/°C available). Resistance tolerance equals ±0.1%. $0.52 (1000). Delivery, eight weeks ARO. **Dale Electronics Inc,** Box 609, Columbus NE 68602. Phone (402) 371-0080. FAX (402) 644-2406. **Circle No. 476**

**Inductors.** D7C and D7F Series inductors are designed for dc/dc-converter and dc/ac-inverter applications. Within both lines, the D73 measures 3.2 mm high; the D75 is 4.8 mm high. The units are available in shielded and unshielded versions. Inductance values are 1 to 100 μH for the 7C units and 1 to 470 μH for 7F units. Current-handling capability ranges from 3A for 1-μH units to 0.5A for 100-μH devices. From $0.66 (1000). **Toko America Inc,** 1250 Feehanville Dr, Mt Prospect, IL 60056. Phone (708) 297-0070. **Circle No. 477**



**Switching transistors.** The MPSH10, MPSH81, and MPS3640 are housed in TO-92 packages. The PMBTH10, PMBTH81, and PMBT3640 are housed in SOT23 cases. The MPSH10/81 and



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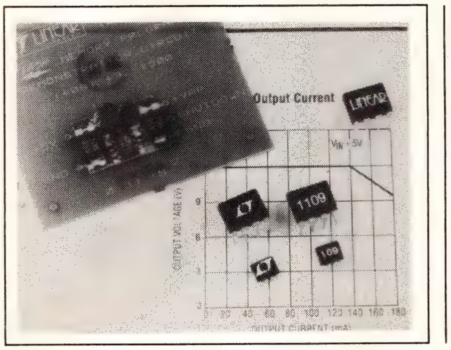
PMBTH10/81 are complementary npn/pnp types. They have a 600-MHz $f_T$, 0.65- and 0.85-pF max collector-base feedback capacitance for the npn and pnp types, respectively, and collector-base time constants of 9 psec. The 3640 units are pnp types that have a 1.5-GHz $f_T$ and 20-nsec switching speeds. PMBTH81, $0.09 (10,000). Delivery, four to eight weeks ARO. **Philips Components,** 2001 W Blue Heron Blvd, Riviera Beach, FL 33404. Phone (800) 447-3762; (407) 881-3308. **Circle No. 478**



**DC/DC converters.** Available in fixed 5V, fixed 12V, and adjustable-voltage versions, the LT1109A is a simple step-up converter that draws 320 µA at no load. The LT1109A-12 device delivers 12V at 140 mA max from a 5V input. The LT1109A-5 develops a 5V/150-mA output from a 2V input. All units feature a logic-controlled shutdown pin that turns the internal oscillator off when the pin goes low. $2.45 (100). Delivery, stock to 60 days ARO. **Linear Technology Corp,** 1630 McCarthy Blvd, Milpitas, CA 95035. Phone (408) 432-1900. FAX (408) 434-0507. **Circle No. 479**

**Rotary switches.** Type 02 switches meet MIL-S-3786/35 requirements. The units are available in 1-pole/12-position or 2-pole/6-position versions. The devices operate over a −40 to +185°F temperature range. They have a 20-mΩ contact resistance and a switch life of 25,000 cycles. The hermetically sealed contacts feature an 80-µin. gold plating. The units are available with solder lugs for panel mounting or tabs for pc-board mounting. From $8.99 (100). **Elma Electronic Inc,** 44350 Grimmer Blvd, Fremont, CA 94538. Phone (510) 656-3400. FAX (510) 656-3783. **Circle No. 480**

**Power dividers.** The SDL Series of 2-, 3-, and 4-way power dividers includes models that cover a frequency range of 2 to 1000 MHz. The devices feature a 0.7-dB typ insertion loss. Additional specifications include an amplitude unbalance of 0.4 dB, typical phase unbalance of 3°, and isolation of 18, 20, and 25 dB between the 4-way, 3-way, and 2-way outputs, respectively. The units are housed in a package measuring 0.31×0.31×0.2 in. $17.95 to $35.95. **Synergy Microwave Corp,** 463 McLean Blvd, Paterson, NJ 07504. Phone (201) 881-8800. FAX (201) 881-8361. **Circle No. 481**

**DC/DC converters.** PJ Series converters develop a 340W output in a package measuring 2×4.25×0.5 in.—80 W/in$^3$. The devices operate with a 155V input and provide outputs of 2.6, 3.3, 5, 12, 15, 24, or 28V. Operating range spans −55 to +85°C. The units feature remote sense, external trim, remote shutdown, and overvoltage and current-limit protection. $573 (100). Delivery, 8 to 10 weeks ARO. **Powercube Corp,** 8 Suburban Park Dr, Billerica, MA 01821. Phone (508) 667-9500. FAX (508) 667-6280. **Circle No. 482**

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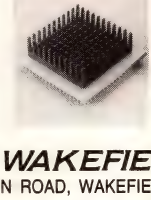
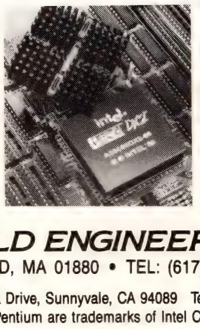
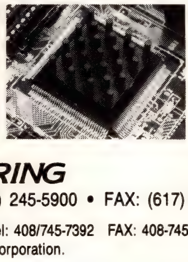

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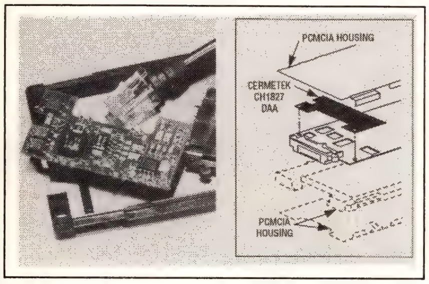

**Line interface.** The CH1827 is a Data Access Arrangement (DAA) that conforms to FCC Part 68. It contains all the traditional DAA functions and works with VFast or V.32bis modems and 14.4-kbaud fax and audio applications. In addition to isolation, the unit features on/off hook control, 2- to 4-wire conversion, ring detect, and surge protection. $15 (OEM qty). **Cermetek Microelectronics Inc,** 1308 Borregas Ave, Sunnyvale, CA 94089. Phone (408) 752-5000. FAX (408) 752-5004. **Circle No. 483**

**DC/DC converters.** Series 1000WFR 10W converters accept inputs of 9 to 72V and develop outputs of 5, 9, 12, 15, ±12, or ±15V. All models include continuous short-circuit protection with automatic restart and an input pi filter. Key specifications include 500V dc isolation, 84% efficiency, output accuracy of ±1%, and a −25 to +71°C operating range. $45 to $48.30 (100). **Conversion Devices Inc,** 15 Jonathan Dr, Brockton, MA 02401. Phone (508) 559-0880. FAX (508) 559-9288. **Circle No. 484**

**DC/DC converters.** The units in this line of single-output 15W converters have a 30-mV p-p output noise. The converters accept 48V inputs and output 5V (Model 48S5.3000TC), 12V (Model 48S12.1250TC), or 15V (Model 48S15.1000TC). Operating range spans −40 to +90°C. All units feature transient/ESD overvoltage protection on the input and output. Overcurrent and overtemperature protection are also standard. $84.53 (100). **Calex Mfg Co Inc,** 2401 Stanwell Dr, Concord, CA 94520. Phone (800) 542-3355; (510) 687-4411. FAX (510) 687-3333. **Circle No. 485**

**Prototyping adapter.** Model ANC-9044 allows you to wire-wrap prototypes that use plastic-leaded-chip-carrier, LCC, or PGA components. The adapters occupy 3 in.$^2$ of board space and provide test points for each of the 44 pins. Adapter pins are on 0.3-in. centered rows to accommodate a variety of prototyping boards. The adapters

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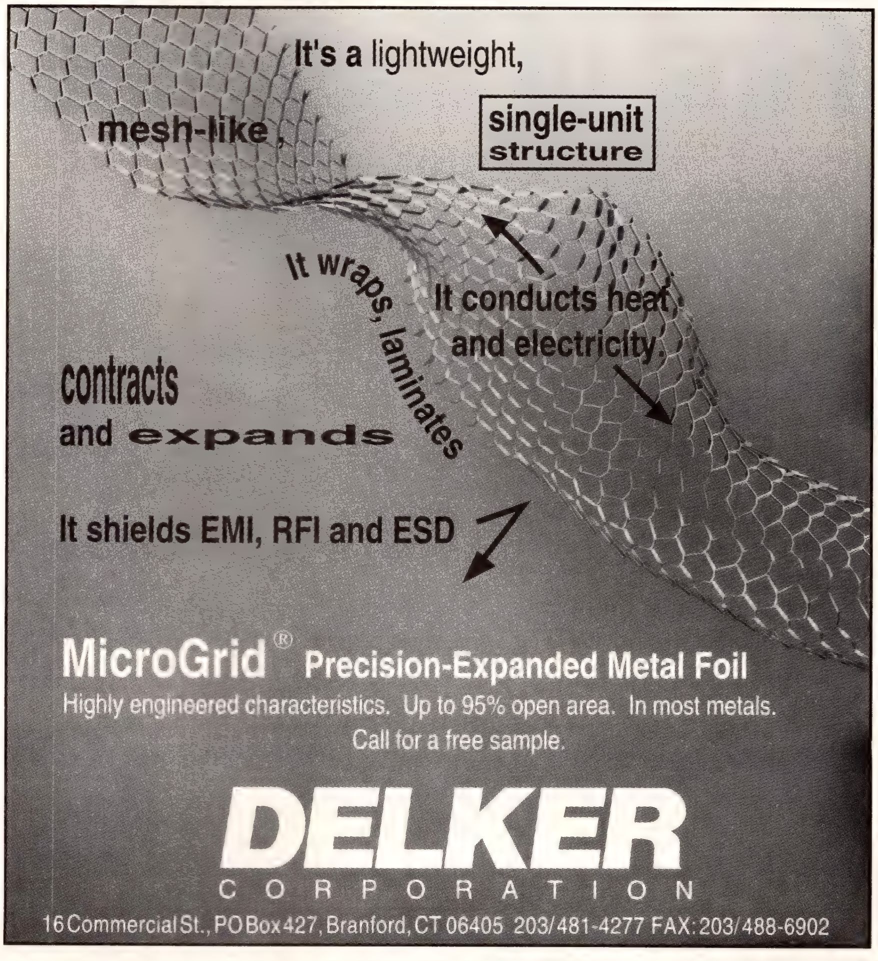
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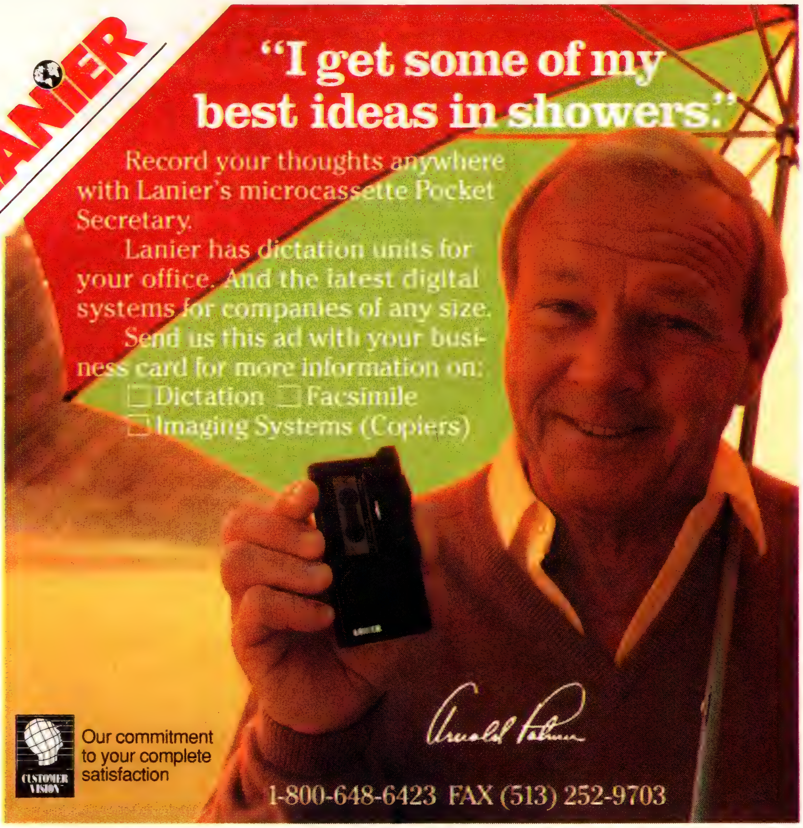

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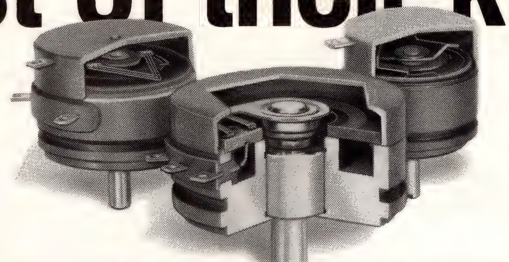

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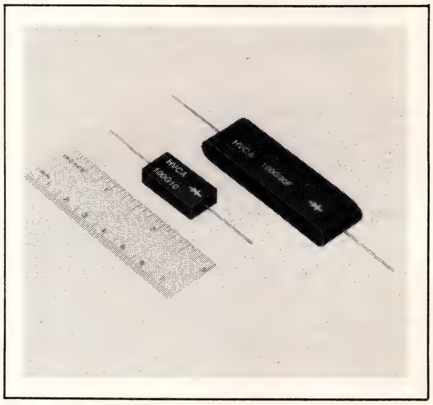
feature two LED status circuits that provide a visual indication of user-selected signals. $36. **Antona Corp,** 1643½ Westwood Blvd, West Los Angeles, CA 90024. Phone (310) 473-8995. FAX (310) 473-7112. **Circle No. 486**



**Rectifier assemblies.** Series 100G silicon rectifiers are available with peak reverse voltage (PRV) ratings of 8000 to 40,000V. Average forward current equals 100 mA, and recovery time measures 250 nsec. Housing for the units measures 1 to 3 in. long, 0.3 to 0.4 in. wide, and 0.5 to 0.75 in. high. $10.25 (100) for a unit with a 20,000V PRV. **HV Component Associates Inc,** Box 2484, Farmingdale, NJ 07727. Phone (908) 938-4499. FAX (908) 938-4451. **Circle No. 487**

**Pushbutton switches.** All models in the SP Series are totally sealed against the entry of harmful contaminants. The line includes spdt and dpdt versions. The snap-action switch mechanism provides tactile response and features a 60,000-cycle electrical life. Various pc-board models have contact current ratings ranging from dry circuit to 1A at 125V ac. $2.95 (1000) for a typical single-pole model. **MORS/ASC,** Box 544, Wakefield, MA 01880. Phone (617) 246-1007. FAX (617) 245-4531. **Circle No. 488**

**Power modules.** The MHW804 Series modules operate over an 806- to 940-MHz frequency range. Both modules in the line operate from a 7.5V supply, have a 50Ω input/output impedance, and develop a 4W output from a 1-mW input. The MHW804-1 unit operates over an 800- to 870-MHz range, and the MHW804-2 version covers the 896- to 940-MHz range. MHW804-1, $50.82; MHW804-2, $52.36 (1-399). **Motorola Inc,** 5005 E McDowell Rd, Phoenix, AZ 85008. Phone (602) 244-3818. FAX (602) 244-4597. **Circle No. 489**

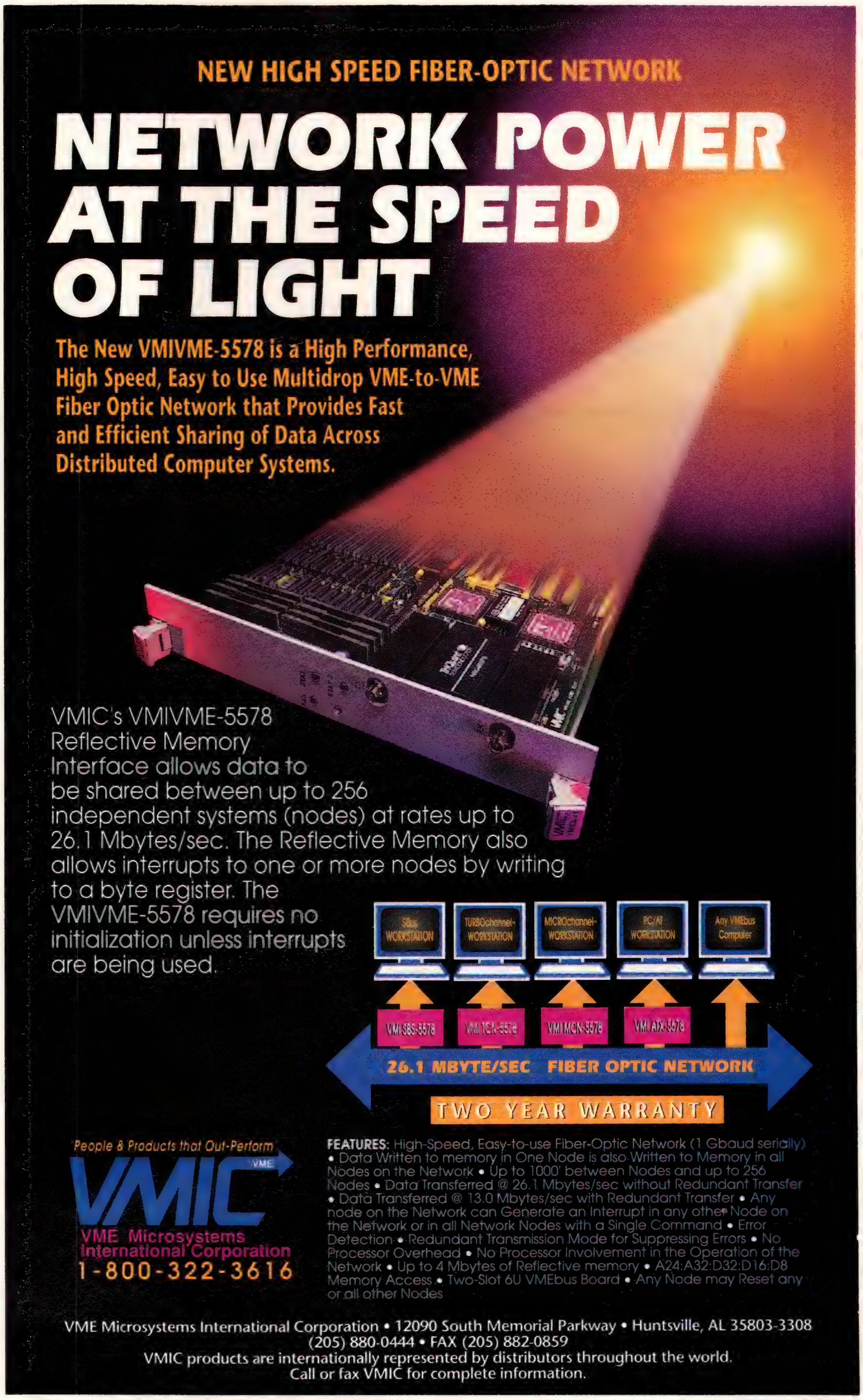
## CAE & Software Development Tools

**Tool for FPGA design and programming.** ALS (Action Logic System) 2.2 adds incremental place and route and an option for interactive placement to the capabilities of previous versions. The added features let you hand-optimize a design after using the tool's automatic place-and-route feature. This release also works with Mentor Graphics 8.2 and OrCAD 4.1 in addition to CAE tools from Viewlogic, Cadence, and Synopsys. For workstation-based development of the maker's Act 1 and Act 2 line of FPGAs, $3995. Interactive Placement option, $1495. **Actel Corp,** 955 E Arques Ave, Sunnyvale, CA 94086. Phone (408) 739-1010. FAX (408) 739-1540. **Circle No. 418**

**RS-232C data-acquisition software.** Softwarewedge reads data from any RS-232C device directly into any PC application. The DOS version is a 5K TSR that captures serial data and transfers it to a foreground program in real time as if it were typed in on the keyboard. The software allows full control over RS-232C input, including data parsing and filtering, date and time stamping, keystroke macro insertion, autoprompting and 2-way serial I/O. The MS-Windows version has all of the features of the DOS version, plus DDE capability. $199. **TAL Enterprises,** 2022 Wallace St, Philadelphia, PA 19130. Phone (800) 722-6004; (215) 763-2620. FAX (215) 763-9711. **Circle No. 419**

**Static code analyzer for Ada, C++, and Fortran.** Metric computes the Software Science and Cyclomatic Complexity series of metrics for code in Ada, C/C++, and Fortran on workstations from HP, IBM, Sun, and 386/486 PCs running Unix. The tool generates reports that include total and unique operators and operands, length vs predicted length, purity ratio, volume, effort, cyclomatic complexity and extended cyclomatic complexity, lines of code, blank lines of code, comment lines of code, and average variable name length. A Summary report combines and extends the previous metrics, and an Exception report lists all program modules that exceed user-defined metric thresholds. $3500 for a 3-user license. **Software Research Inc,** 625 Third St, San Francisco, CA 94107. Phone (800) 942-7638; (415) 957-1441 FAX (415) 957-0730. **Circle No. 420**

**Tools for analog and digital design.** Design Center 5.3 adds many features to previous versions. Features include an interface to the PADS and Protel board layout packages; device-temperature customizing; histograms; multiple-plot windows for waveform analysis; hardcopy enhancements; tracking and display of simulator-generated condition messages; editing of model definitions in the schematic capture program to support Monte Carlo analysis; and a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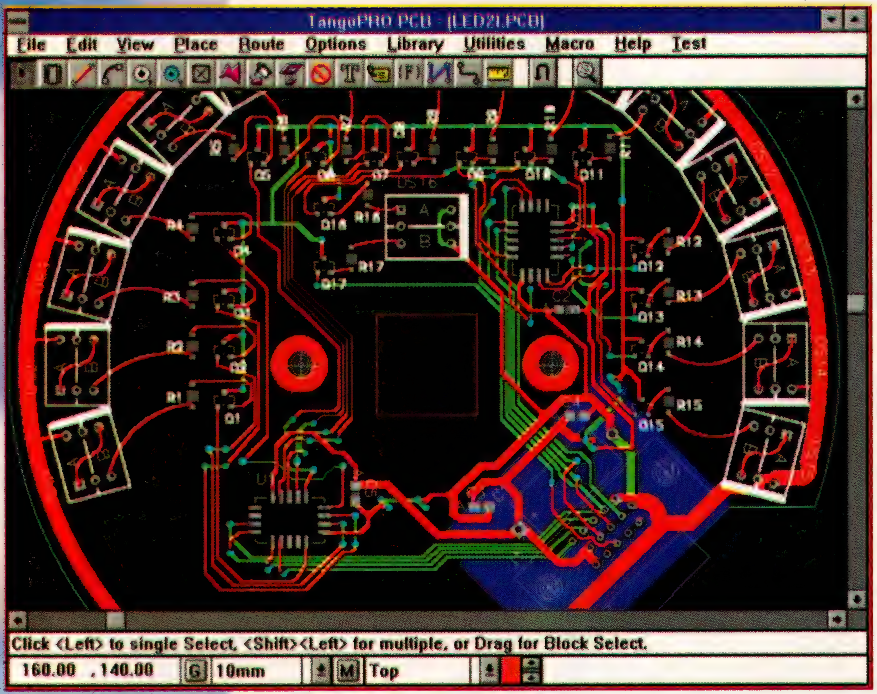

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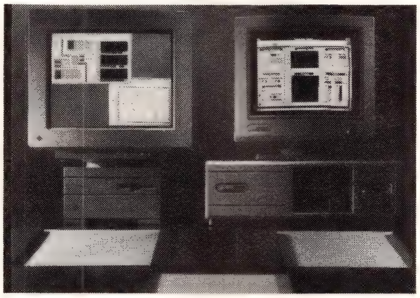
**Timing software for AMD 29K and Cypress PLDs.** Interactive Data Books is interactive-timing-analysis software that initially covers the AMD 29K family of RISC (reduced-instruction-set-computer) microprocessors and PLDs from Cypress Semiconductor. The software contains both electronically readable timing data and complete electronically manipulable timing diagrams for specific devices. You view the diagrams with an included tool called Timingviewer, which is a read-only version of the makers' interactive-timing-analysis software. You can also use the timing data with most spreadsheet software. $49 each for AMD 29K and Cypress PLDs. **Chronology Corp,** 2721 152nd Ave NE, Redmond, WA 98052. Phone (206) 869-4227. FAX (206) 869-4229. **Circle No. 422**

**Neural networks on Lotus 1-2-3.** The @BRAIN Neural Network Development System lets you embed neural networks in Lotus 1-2-3 spreadsheets. The system is both mathematically and numerically stable, converges to a solution quadratically, and requires no learning parameters. The system includes data entry using a dialog box, automatic detection of CPU type and automatic network configuration, a virtual memory manager that handles large networks, and an unlimited number of networks per spreadsheet. The system should be available for Microsoft Excel by the end of this quarter. $495. **Talon Development Corp,** Box 11069, Milwaukee, WI 53211. Phone (414) 962-7246. **Circle No. 423**

**Virtual instrument software for PCs and SPARCstations.** Labview is a general-purpose programming tool with extensive libraries for data acquisition, instrument control, data analysis, and data presentation. Originally designed for Macintosh, with this release the software also runs on PCs and SPARCstations. The software includes a library of ready-to-use controls, graphs, and strip charts and tools to build block diagrams as executable programs. The software also includes icon libraries and drivers for 100 IEEE-488, VXI, and RS-232C instruments using the maker's interface hardware, as well as analysis virtual instrument libraries for performing data analysis ranging from statistics to digital signal processing. PC version, $1995; SPARC version, $3995. **National Instruments,** 6504 Bridge Point Pkwy, Austin, TX 78730. Phone (800) 433-3488; (512) 794-0100. FAX (512) 794-8411. **Circle No. 424**



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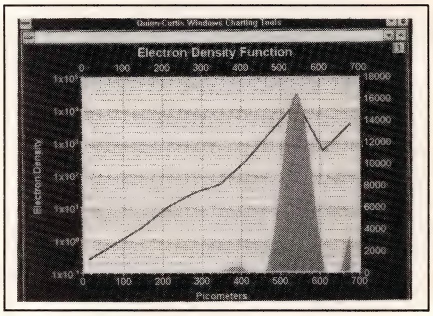
**Assembler development tools for 80x86.** MASM (Microsoft Macro Assembler Professional Development System) 6.1 gives you instruction timings; a broader selection of high-level directives; documentation on programming for Windows; improved code compatibility with MASM 5.1; ability to target Windows NT, DOS, and MS-Windows; remote debugging; C++ debugging; and a faster edit/assemble/link cycle. Documentation runs to 1500 pages in both on-line and print form. $199. **Microsoft Corp,** 1 Microsoft Way, Redmond, WA 98052. Phone (206) 882-8080. FAX (206) 936-7329. TLX 160520. **Circle No. 425**

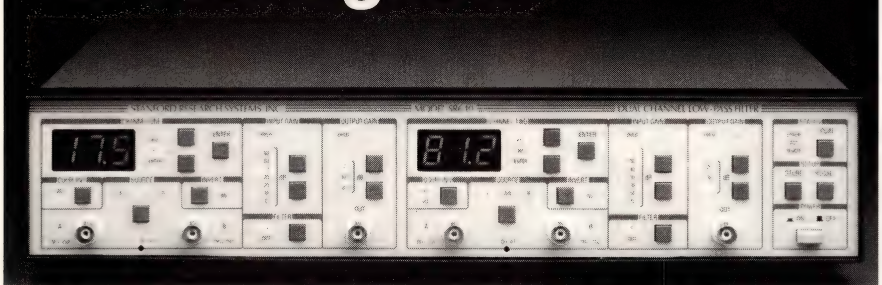
**Real-time metrics on pSOS.** The RTOS Measurement Tool lets users see real-time views of operating system behavior in embedded systems. Used with the HP64700 series emulators and HP's graphical debugger, this tool shows system activity flow, software timing profiles and dynamic memory usage, in addition to measurements that isolate software defects. Runs on HP 9000 and Sun SPARCstations and targets Motorola 68000 series processors. From $2500. **Integrated Systems Inc,** 3260 Jay St, Santa Clara, CA 95054. Phone (408) 980-1500. FAX (408) 980-0400. **Circle No. 426**



**Charting tools for C/C++.** Windows Charting Tools is a collection of general-purpose graphics and user-interface routines that solve most common charting problems. The software works with Microsoft C/C++ and Borland C++ under MS-Windows 3.1. Structured as a library of C functions, the software produces presentation-quality output on devices ranging from dot-matrix through laser printers to typesetting equipment. For the PC, from $400. **Quinn-Curtis,** 35 Highland Circle, Needham, MA 02194. Phone (617) 449-6155. FAX (617) 449-6109. **Circle No. 427**

**Signal-processing library for C++.** The Signal++ signal-processing library lets you simulate, test, and generate signal-processing algorithms using C++. The library gives you discrete-time signal and noise simulations, digital signal processing, digital and analog filter designs, time-domain correlations, filtering, and FFTs. The library includes an interface to user-written programs. Available for most PC C++ compilers and for several memory models, including some DOS extenders. From $99. **Sigsoft,** 15865 Lofty Trail Dr, San Diego, CA 92127. Phone (619) 673-0745. **Circle No. 428**

**Automated testing for NT.** Testrunner for NT is a nonintrusive, automated software-testing tool that records operator input, then replays it, comparing performance with a stored file of expected results. The tool synchronizes it-



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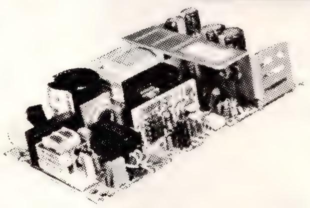

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**Gate-array design kit for DEC Alpha.** FX Gate Array Kit lets you design GaAs ASICs using Digital Equipment Corp's 64-bit Alpha AXP RISC (reduced-instruction-set-computer) system. The FX Series consists of five gate arrays ranging from 20,000 to 350,000 raw gates. The kit includes macrocell libraries and software tools required to design, simulate, and analyze a circuit. You can use it for schematic capture and simulation with tools from Viewlogic, Cadence, or Mentor. The kit also includes tools for performance calculations, design rule checks, front- and back-annotated wire length, RC delay estimates, macrocell preplacement, and test-vector analysis. No charge for users who design ASICs targeted at the process. **Vitesse Semiconductor Inc**, 741 Calle Plano, Camarillo, CA 93012. Phone (805) 388-3700. **Circle No. 433**

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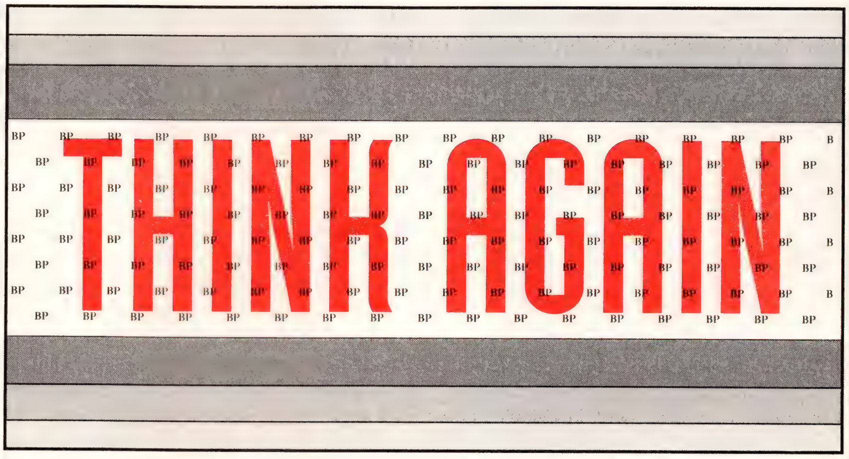

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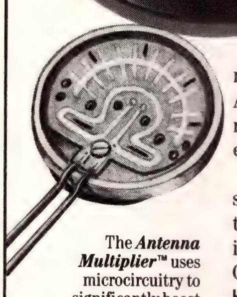

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**Brochure on rubber-sheet keyboard.** The 2-pg color brochure describes the G83-3000 keyboard featuring membrane switch contacts with a single rubber sheet. According to the brochure, the 101-key keyboard is compatible with the IBM PC/AT and PS/2 computers. **Cherry Electrical Products,** 3600 Sunset Ave, Waukegan, IL 60087. Phone (708) 360-3599. **Circle No. 415**

**Three app notes on motion control.** *AN-230, Circuit Applications of the AD2S90 Resolver-to-Digital Converter* explains the flexibility of the AD2S90 12-bit monolithic resolver-to-digital converter (RDC). It demonstrates how to interface the converter's absolute serial output to standard parallel buses and EIA-485 balanced, serial communications receivers. *AN-234, Digital Resolver Integration* describes the integration of the AD2S90 RDC and support circuitry onto a size 11 resolver to produce a virtual digital resolver—a resolver with digital position output as well as a Quad B encoder-emulated output. *AN-236, Speed Measurement and Control with the AD2S83, a "Silicon Tachogenerator"* describes implementation of the AD2S83 RDC to provide accurate velocity output with improved performance and greater reliability than a discrete tachogenerator. **Analog Devices Inc,** 181 Ballardvale St, Wilmington, MA 01887. Phone (617) 937-1428. **Circle No. 416**

**Catalog of EMI shielding products.** This 156-pg book is divided into nine tabulated product sections. It covers a line of conductive materials, including knitted wire mesh, metal fibers, screens, oriented wires in elastomers, shielding windows, and several other shielding products. The catalog also highlights the products that are shipped within 24 hours. **Tecknit,** 129 Dermody St, Cranford, NJ 07016. Phone (908) 272-5500. **Circle No. 417**

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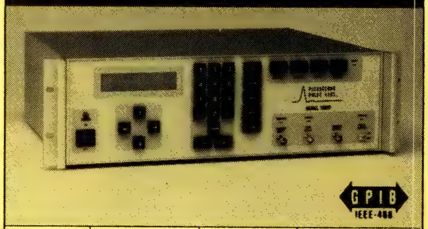

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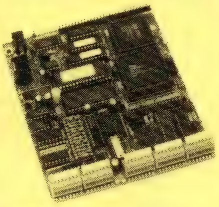

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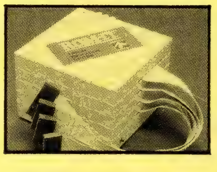

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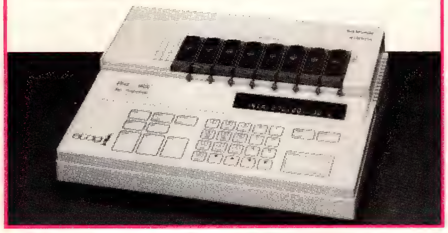

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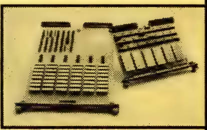

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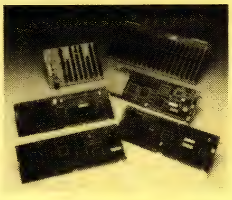

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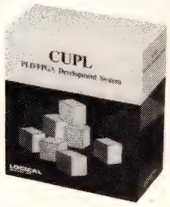

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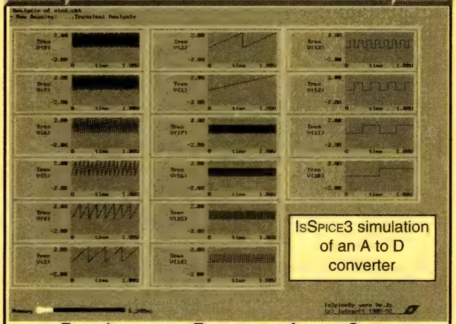

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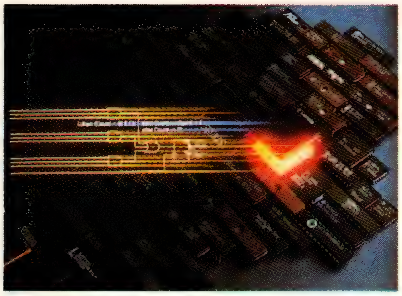

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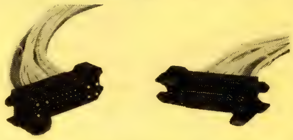

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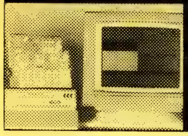

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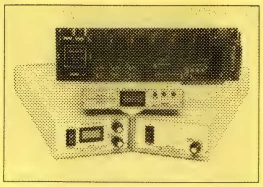

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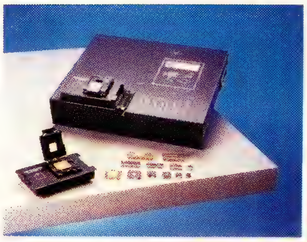

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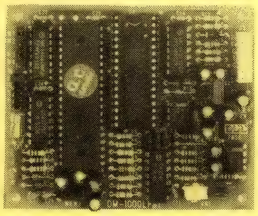

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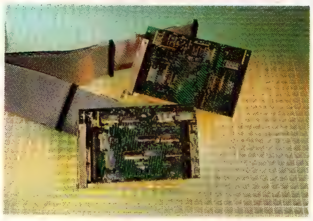

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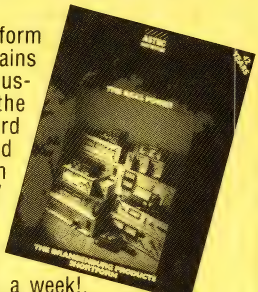

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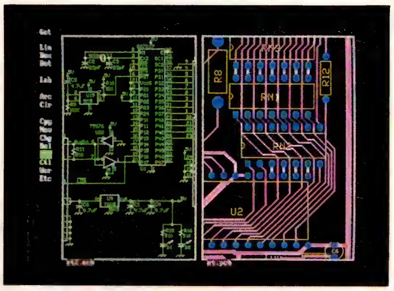

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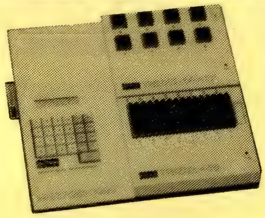

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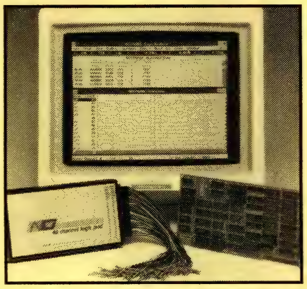

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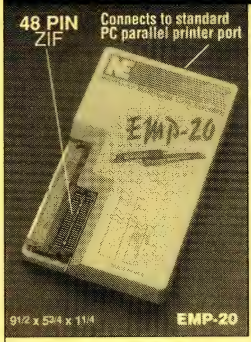

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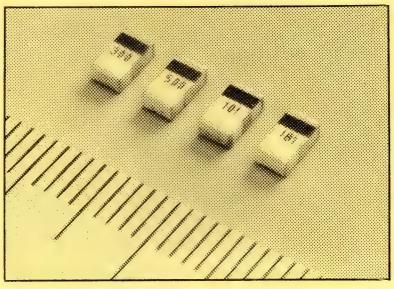

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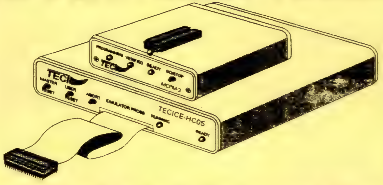

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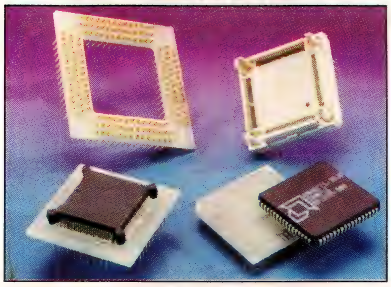

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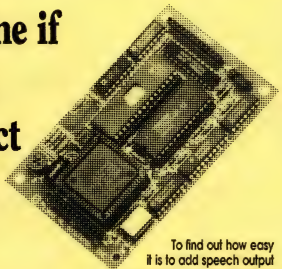

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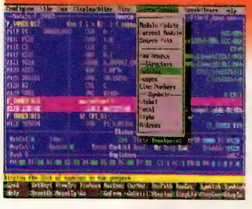

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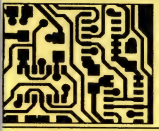

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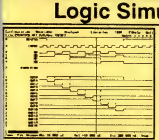

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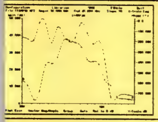

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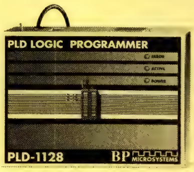

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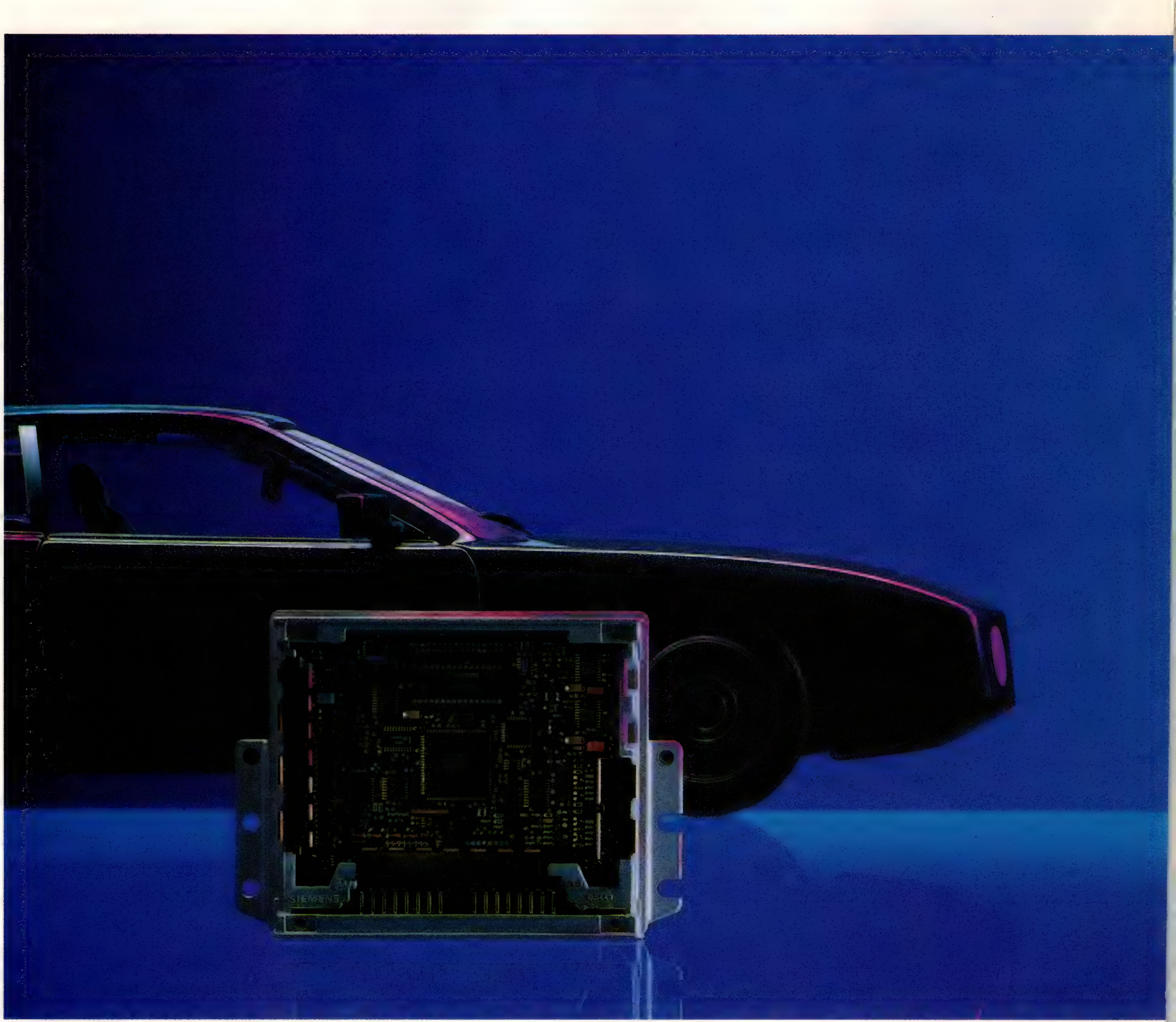

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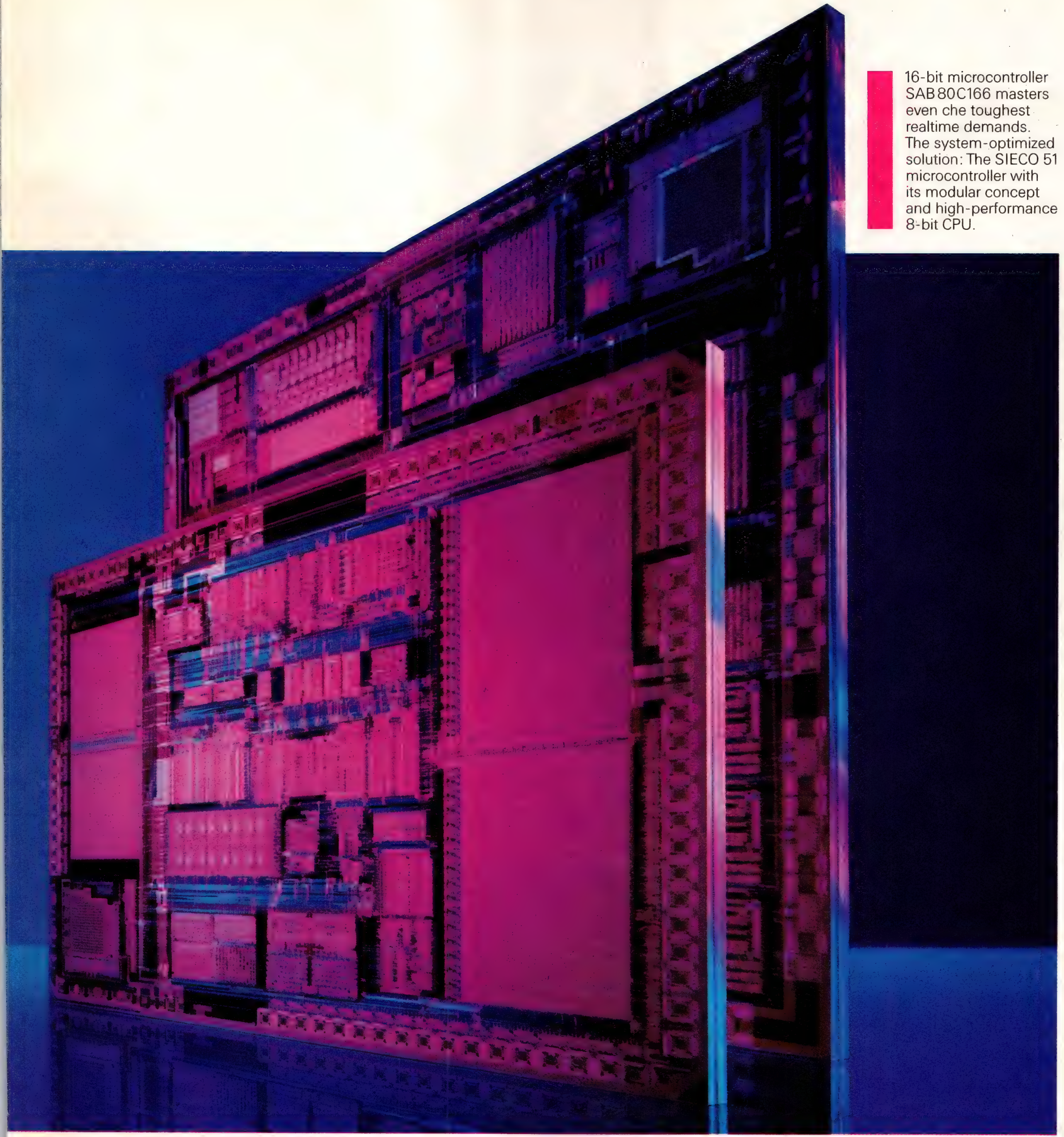
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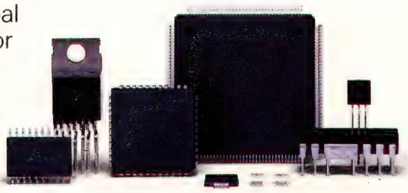

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